



PNX8526

Programmable source decoder with integrated peripherals

Rev. 01 – 6 October 2003

Preliminary data

1. General description

The PNX8526 is a highly integrated media processor for use in Advanced Set Top Boxes (ASTB) and Digital Television (DTV) systems. The PNX8526 is targeted at the mid to high-end ASTB/DTV systems, decoding “all format” HD and SD MPEG2 source material with Standard Definition (SD), or double line-rate SD display capabilities. Although the PNX8526 can process high level input formats, its display capabilities are primarily targeted at NTSC, PAL and SECAM televisions. It is also intended for lower cost DTVs, those not considered high definition. Progressive output is also available for double line-rate television displays, or for high resolution graphic content to be displayed on a computer monitor. The PNX8526 is designed in a high performance 0.12-micron process.

The PNX8526 performs source decode functions, including - conditional access, MPEG2 transport stream de-mux, MPEG2 video decode, audio decode and processing, graphics generation, video processing, and image composition and display. A 32-bit 200 MHz VLIW processor, referred to as the TriMedia™ 3200 CPU core (TM32 CPU), carries out the majority of media processing operations performed by the PNX8526. Fixed function hardware will perform some operations that are not handled by the TM32 CPU. Additionally, the PNX8526 supports a number of peripheral interfaces such as I²C, USB, IDE and UART. Other interfaces such as IEEE-1284 and Ethernet may be supported via Super I/O devices that reside on a PCI expansion bus. The expansion bus also provides for glueless interface to 8-bit wide slave devices, such as Flash/ROM, DOCSIS modem, UARTs, etc.

An embedded MIPS processor (PR3940) running at 150 MHz is intended to run the OS. (There is no direct support for an external processor; however, a CPU of any type may be connected to the PNX8526 via the PCI interface.) This implies a complete CPU subsystem consisting of the CPU itself, local memory, and an interface to PCI. The MIPS processor is primarily responsible for control functions and graphics-intensive operating systems, while the TM32 CPU is responsible for running all real-time media processing functions. All resources supported within the PNX8526 are accessible by both the MIPS processor and the TM32 CPU. The software documentation of the PNX8526 provides more details on the interaction between the MIPS and the TM32 CPU.

The PNX8526 is intended to be used with a small companion IC, the PNX8510. This analog companion chip provides the majority of analog video and audio support for the output of the PNX8526. The PNX8510 companion is capable of simultaneously driving two video channels (6 DACs) and two stereo audio channels (4 DACs).



PHILIPS

2. Features

- 200 MHz, 5 instruction/clock cycle 32-bit VLIW processing core (TM32 CPU)
- 150 MHz, MIPS PR3940 processing core
- External CPU support via PCI
- Support for multiple digital video (D1) input streams
- Support for multiple MPEG2 or DIRECTV transport streams (parallel format)
- On-chip conditional access for DVB, DES, MULTI2, CAM, DIRECTV
- On-chip copy protection support for OpenCable™ and ATSC (NRSS-B)
- Simultaneous decode of two SD streams (MPEG2) or one HD MPEG Stream (AFD style HD-SD decode)
- Simultaneous decode of two AC-3 or equivalent audio streams
- High performance 2D rendering and DMA capability
- Dual image composition/screen refresh engines: four layer primary output, two layer secondary output
- Multiple channel output to support watch/record and multi-room modes
- Embedded 1394 link layer with 5C copy protection
- Soft modem support via SSI interface
- 16, 32, and 64 MB Unified Memory Architecture implemented with high speed SDRAM (166 MHz)
- System expansion capability via industry standard PCI bus
- Core peripherals (I²C, UART, USB, etc.) on the chip, other peripherals supported via third-party SuperIO chip

3. Applications

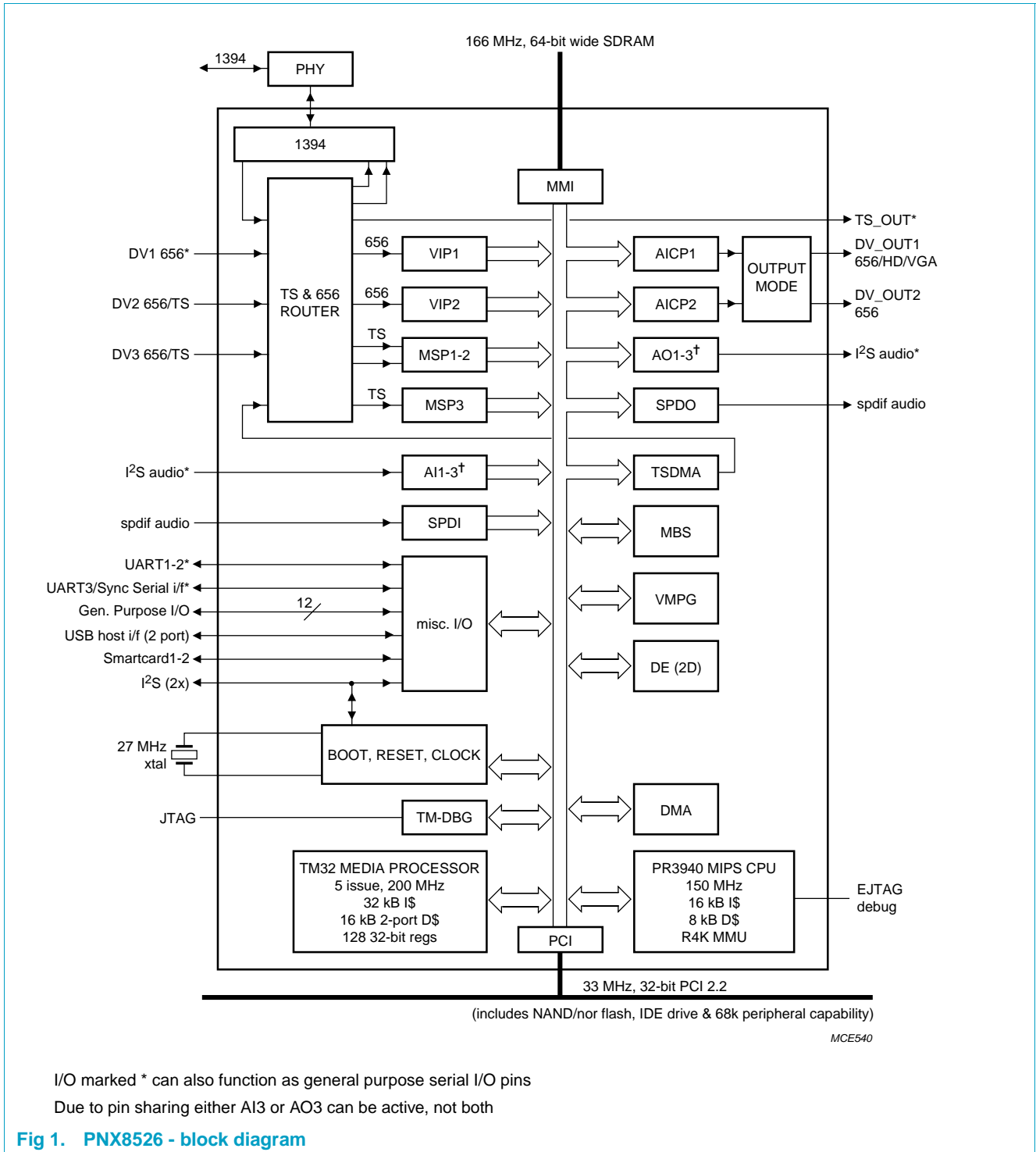
- Advanced Set Top Box (ASTB)
- Digital Television (DTV)

4. Ordering information

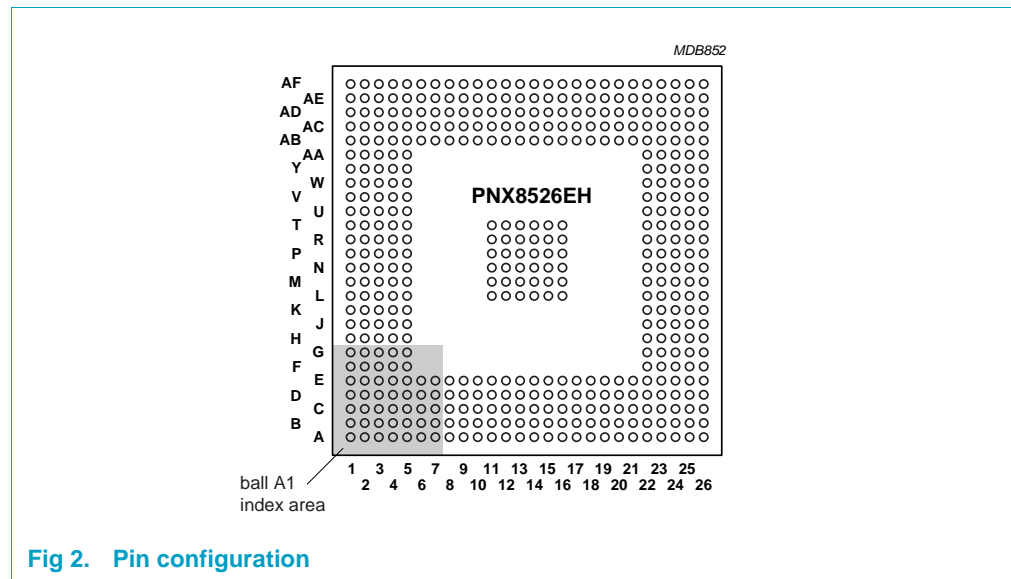
Table 1: Ordering Information

Type number	Package Name	Description	Version
PNX8526EH	HBGA456	Plastic thermal enhanced ball grid array package; 456 balls; body 35 x 35 x 1.8 mm; heatsink	SOT610-1

5. Block diagram



6. Pinning information



6.1 Pinning

In the tables that follow the PNX8526 signals have been sorted by functional group. For quick reference, [Table 2](#) identifies each functional group and gives table location.

Table 2: Signal groups

Functional Group	Group Name	Table/Page Number
PCI	Peripheral Controller Interface	Table 3 on page 5
MISC	Miscellaneous System Interface	Table 4 on page 7
MMI	Main Memory Interface	Table 5 on page 7
GPIO	General Purpose Input/Output	Table 6 on page 9
COM	Serial Communication	Table 7 on page 10
USB	Universal Serial Bus	Table 8 on page 10
1394	IEEE 1394 Port	Table 9 on page 11
I ² C-bus	Serial Communications Port	Table 10 on page 11
AVIF	Audio and Video Interface	Table 11 on page 11
DVB	Digital Video Bus	Table 12 on page 13
PLL	Phase Lock Loop	Table 13 on page 14
PWR	Analog Power and Ground / Digital Power and Ground Connections	Table 14 on page 14
TEST	Test Contacts	Table 15 on page 17
All pins	Pin Descriptions in alpha/numeric order	Table 16 on page 18

6.2 Pin description

All pad inputs and I/O have built-in pull-ups (~80 kΩ) and Schmitt trigger input thresholds. (See [Table 19](#) for maximum ratings).

The following pins do not have pull-ups:

XTALI, PC1x, analog pins, I²C, Main Memory Interface, USB_DPx and USB_DMx.

The following pins do not have Schmitt trigger inputs:

XTALI, analog pins, USB_DPx and USB_DMx.

Table 3: Peripheral Controller Interface (PCI)

indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
AD[31]	AB1	I/O	Multiplexed Address or Data Bit 31	
AD[30]	AB2	I/O	Multiplexed Address or Data Bit 30	
AD[29]	AB3	I/O	Multiplexed Address or Data Bit 29	
AD[28]	AB4	I/O	Multiplexed Address or Data Bit 28	
AD[27]	AC1	I/O	Multiplexed Address or Data Bit 27	
AD[26]	AC2	I/O	Multiplexed Address or Data Bit 26	
AD[25]	AC3	I/O	Multiplexed Address or Data Bit 25	
AD[24]	AD2	I/O	Multiplexed Address or Data Bit 24	
AD[23]	AE3	I/O	Multiplexed Address or Data Bit 23	
AD[22]	AF4	I/O	Multiplexed Address or Data Bit 22	
AD[21]	AE4	I/O	Multiplexed Address or Data Bit 21	
AD[20]	AD4	I/O	Multiplexed Address or Data Bit 20	
AD[19]	AE5	I/O	Multiplexed Address or Data Bit 19	
AD[18]	AD5	I/O	Multiplexed Address or Data Bit 18	
AD[17]	AC5	I/O	Multiplexed Address or Data Bit 17	
AD[16]	AC6	I/O	Multiplexed Address or Data Bit 16	
AD[15]	AD8	I/O	Multiplexed Address or Data Bit 15	
AD[14]	AC8	I/O	Multiplexed Address or Data Bit 14	
AD[13]	AF9	I/O	Multiplexed Address or Data Bit 13	
AD[12]	AE9	I/O	Multiplexed Address or Data Bit 12	
AD[11]	AD9	I/O	Multiplexed Address or Data Bit 11	
AD[10]	AC9	I/O	Multiplexed Address or Data Bit 10	
AD[09]	AF10	I/O	Multiplexed Address or Data Bit 9	
AD[08]	AE10	I/O	Multiplexed Address or Data Bit 8	
AD[07]	AC10	I/O	Multiplexed Address or Data Bit 7	
AD[06]	AF11	I/O	Multiplexed Address or Data Bit 6	
AD[05]	AE11	I/O	Multiplexed Address or Data Bit 5	
AD[04]	AD11	I/O	Multiplexed Address or Data Bit 4	
AD[03]	AC11	I/O	Multiplexed Address or Data Bit 3	
AD[02]	AE12	I/O	Multiplexed Address or Data Bit 2	
AD[01]	AD12	I/O	Multiplexed Address or Data Bit 1	
AD[00]	AC12	I/O	Multiplexed Address or Data Bit 0	
C/BE[3]	AD1	I/O	Multiplexed Command or Byte Enable 3	
C/BE[2]	AF5	I/O	Multiplexed Command or Byte Enable 2	

Table 3: Peripheral Controller Interface (PCI)...*continued*# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
C/ $\overline{\text{BE}}[1]$	AE8	I/O	Multiplexed Command or Byte Enable 1	
C/ $\overline{\text{BE}}[0]$	AD10	I/O	Multiplexed Command or Byte Enable 0	
CLK	AA1	I	PCI Bus Clock	
DEVSEL	AF7	I/O	Device Select is asserted when a target address is decoded and remains asserted to indicate that a target device is selected.	
FRAME	AF6	I/O	Frame is asserted to indicate start of bus transaction and remains asserted until final data phase begins.	
GNT	Y3	I/O	Arbitration Grant is asserted to indicate access to the bus has been granted. This pin is an input when an external arbiter is used and an output when using the internal arbiter.	
GNT_A	Y4	I/O	Auxiliary Arbitration Grant_A is asserted to indicate bus access has been granted to an external PCI master. Used where internal arbiter is configured.	#
GNT_B	AA4	I/O	Auxiliary Arbitration Grant_B is asserted to indicate bus access has been granted to an external PCI master. Used where internal arbiter is configured.	#
IDSEL	AF3	I/O	Initialization Device Select provides chip select during configuration read and write transactions.	
INTA	V4	I/O	Interrupt A is asserted to request an interrupt. This pin may be configured as an input if the internal PIC is used, or as an output if the external interrupt controller is used. Polarity in active low.	
IRDY	AE6	I/O	Initiator Ready is asserted during writes to indicate valid data on AD[31:0]. Also asserted during reads to indicate the target is prepared to accept data. Wait states are inserted until IRDY and TRDY are both asserted.	
PAR	AF8	I/O	Parity supports even parity across the PCI Address/Data Bus AD[31:0]) and Command/Byte Enable Bus (C/ $\overline{\text{BE}}[3:0]$). The Bus Master drives PAR for address and write data phases. The Target drives PAR for the read data phases.	
PERR	AD7	I/O	Parity Error indicates data parity errors during all PCI transactions except Special Cycle.	
REQ	Y2	I/O	Arbitration Request on PCI Bus. Request is an output when using an external arbiter and an input when using an internal arbiter.	
REQ_A	AA2	I/O	Auxiliary Arbitration REQ_A on PCI Bus. Used in modes where internal arbiter is configured.	#
REQ_B	AA3	I/O	Auxiliary Arbitration REQ_B on PCI Bus. Used in modes where internal arbiter is configured.	#
RESET_IN	W3	I	PCI Bus Global Reset	
SERR	AC7	I/O	System Error	
STOP	AE7	I/O	Stop is asserted to indicate a request from the target for the master to stop the current transmission.	
TRDY	AD6	I/O	Target Ready is asserted during reads to indicate valid data on AD[31:0]. It is asserted during writes to indicate the target is prepared to accept data. Wait states are inserted until IRDY and TRDY are both asserted.	

Table 4: Misc. System Interface (MISC)# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
XIO_A25	AE13	I/O	XIO Address Bit 25	#
XIO_ACK	AF13	I/O	XIO Acknowledge (EEPROM)	#
XIO_SEL[2]	AF12	I/O	External I/O Select2	#
XIO_SEL[1]	AC13	I/O	External I/O Select1	#
XIO_SEL[0]	AD13	I/O	External I/O Select0	#
SYS_RSTN_OUT	Y1	O	System Reset Output	#

Table 5: Main Memory Interface (MMI)# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
MA[11]	C22	O	Memory Address Bit 11	
MA[10]	B21	O	Memory Address Bit 10	
MA[9]	A21	O	Memory Address Bit 9	
MA[8]	C21	O	Memory Address Bit 8	
MA[7]	A20	O	Memory Address Bit 7	
MA[6]	C20	O	Memory Address Bit 6	
MA[5]	D18	O	Memory Address Bit 5	
MA[4]	D19	O	Memory Address Bit 4	
MA[3]	C19	O	Memory Address Bit 3	
MA[2]	D20	O	Memory Address Bit 2	
MA[1]	B20	O	Memory Address Bit 1	
MA[0]	D21	O	Memory Address Bit 0	
MD[63]	M25	I/O	Memory Data Bit 63	
MD[62]	M24	I/O	Memory Data Bit 62	
MD[61]	M23	I/O	Memory Data Bit 61	
MD[60]	L26	I/O	Memory Data Bit 60	
MD[59]	L25	I/O	Memory Data Bit 59	
MD[58]	L24	I/O	Memory Data Bit 58	
MD[57]	L23	I/O	Memory Data Bit 57	
MD[56]	K26	I/O	Memory Data Bit 56	
MD[55]	K24	I/O	Memory Data Bit 55	
MD[54]	K23	I/O	Memory Data Bit 54	
MD[53]	J26	I/O	Memory Data Bit 53	
MD[52]	J25	I/O	Memory Data Bit 52	
MD[51]	J24	I/O	Memory Data Bit 51	
MD[50]	J23	I/O	Memory Data Bit 50	
MD[49]	H26	I/O	Memory Data Bit 49	
MD[48]	H25	I/O	Memory Data Bit 48	
MD[47]	H23	I/O	Memory Data Bit 47	

Table 5: Main Memory Interface (MMI)...*continued*# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
MD[46]	G26	I/O	Memory Data Bit 46	
MD[45]	G25	I/O	Memory Data Bit 45	
MD[44]	G24	I/O	Memory Data Bit 44	
MD[43]	G23	I/O	Memory Data Bit 43	
MD[42]	F26	I/O	Memory Data Bit 42	
MD[41]	F25	I/O	Memory Data Bit 41	
MD[40]	F24	I/O	Memory Data Bit 40	
MD[39]	F23	I/O	Memory Data Bit 39	
MD[38]	E25	I/O	Memory Data Bit 38	
MD[37]	E24	I/O	Memory Data Bit 37	
MD[36]	D25	I/O	Memory Data Bit 36	
MD[35]	D26	I/O	Memory Data Bit 35	
MD[34]	E23	I/O	Memory Data Bit 34	
MD[33]	D24	I/O	Memory Data Bit 33	
MD[32]	C25	I/O	Memory Data Bit 32	
MD[31]	A18	I/O	Memory Data Bit 31	
MD[30]	B18	I/O	Memory Data Bit 30	
MD[29]	C18	I/O	Memory Data Bit 29	
MD[28]	A19	I/O	Memory Data Bit 28	
MD[27]	B17	I/O	Memory Data Bit 27	
MD[26]	C17	I/O	Memory Data Bit 26	
MD[25]	D17	I/O	Memory Data Bit 25	
MD[24]	A16	I/O	Memory Data Bit 24	
MD[23]	B16	I/O	Memory Data Bit 23	
MD[22]	C16	I/O	Memory Data Bit 22	
MD[21]	D16	I/O	Memory Data Bit 21	
MD[20]	A15	I/O	Memory Data Bit 20	
MD[19]	B15	I/O	Memory Data Bit 19	
MD[18]	C15	I/O	Memory Data Bit 18	
MD[17]	D15	I/O	Memory Data Bit 17	
MD[16]	C14	I/O	Memory Data Bit 16	
MD[15]	A14	I/O	Memory Data Bit 15	
MD[14]	D14	I/O	Memory Data Bit 14	
MD[13]	A13	I/O	Memory Data Bit 13	
MD[12]	B13	I/O	Memory Data Bit 12	
MD[11]	C13	I/O	Memory Data Bit 11	
MD[10]	D13	I/O	Memory Data Bit 10	
MD[09]	A12	I/O	Memory Data Bit 09	
MD[08]	B12	I/O	Memory Data Bit 08	

Table 5: Main Memory Interface (MMI)...*continued*# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
MD[07]	C12	I/O	Memory Data Bit 07	
MD[06]	A11	I/O	Memory Data Bit 06	
MD[05]	B11	I/O	Memory Data Bit 05	
MD[04]	D11	I/O	Memory Data Bit 04	
MD[03]	A10	I/O	Memory Data Bit 03	
MD[02]	C11	I/O	Memory Data Bit 02	
MD[01]	B10	I/O	Memory Data Bit 01	
MD[00]	C10	I/O	Memory Data Bit 00	
MDQM[7]	K25	O	SDRAM Control Bit 7	
MDQM[6]	H24	O	SDRAM Control Bit 6	
MDQM[5]	E26	O	SDRAM Control Bit 5	
MDQM[4]	A24	O	SDRAM Control Bit 4	
MDQM[3]	A17	O	SDRAM Control Bit 3	
MDQM[2]	B14	O	SDRAM Control Bit 2	
MDQM[1]	D12	O	SDRAM Control Bit 1	
MDQM[0]	A9	O	SDRAM Control Bit 0	
MBA[1]	D22	O	SDRAM Bank Select	
MBA[0]	B22	O	SDRAM Bank Select	
MCKE	C23	O	Memory Clock Enable	
MCLK[1]	C26	O	Memory Clock	
MCLK[0]	B19	O	Memory Clock	
MCS	A22	O	Memory Chip Select	
MRAS	B23	O	EDODRAM Row Address Strobe	
MCAS	A23	O	Memory Column Address Select	
MWE	B24	O	Memory Write Enable	

Table 6: General Purpose Input/Output (GPIO)# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
GPIO[11]	N26	I/O	General Purpose Input/Output Bit 11	#
GPIO[10]	N24	I/O	General Purpose Input/Output Bit 10	#
GPIO[9]	N23	I/O	General Purpose Input/Output Bit 9	#
GPIO[8]	M26	I/O	General Purpose Input/Output Bit 8	#
GPIO[7]	AE14	I/O	General Purpose Input/Output Bit 7	#
GPIO[6]	AF14	I/O	General Purpose Input/Output Bit 6	#
GPIO[5]	AD14	I/O	General Purpose Input/Output Bit 5	#
GPIO[4]	AC14	I/O	General Purpose Input/Output Bit 4	#
GPIO[3]	C5	I/O	General Purpose Input/Output Bit 3	#

Table 6: General Purpose Input/Output (GPIO)...continued# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
GPIO[2]	B4	I/O	General Purpose Input/Output Bit 2	#
GPIO[1]	D5	I/O	General Purpose Input/Output Bit 1	#
GPIO[0]	C4	I/O	General Purpose Input/Output Bit 0	#

Table 7: Serial Communication (COM)# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
UA1_TX	U24	I/O	UART1 Transmit	#
UA1_RX	U25	I/O	UART1 Receive	#
UA2_TX	T23	I/O	UART2 Transmit	#
UA2_RX	U26	I/O	UART2 Receive	#
UA2_RTSN	T24	I/O	UART2 Request To Send	#
UA2_CTSN	T25	I/O	UART2 Clear To Send	#
SC1_DA	T26	I/O	Smart Card1 Data	
SC1_CMD	R23	O	Smart Card1 Command	
SC1_RST	R24	O	Smart Card1 Reset	
SC1_OFFN	R25	I	Smart Card1 Off	
SC1_SCCK	R26	O	Smart Card1 Bit Clock	
SC2_DA	P23	I/O	Smart Card2 Data	
SC2_CMD	P24	O	Smart Card2 Command	
SC2_RST	P26	O	Smart Card2 Reset	
SC2_OFFN	P25	I	Smart Card2 Off	
SC2_SCCK	N25	O	Smart Card2 Bit Clock	
SSI_SCLK_CTSN	V1	I/O	Synchronous Serial Interface Clock Input	#
SSI_FS_RTSN	V2	I/O	Synchronous Serial Interface Frame Sync	#
SSI_RXD	U4	I/O	Synchronous Serial Interface Receive	#
SSI_TXD	V3	I/O	Synchronous Serial Interface Transmit	#

Table 8: Universal Serial Bus (USB)

Symbol	Pin	Type	Description
USB_DP[1]	A5	I/O	Data Plus Bit 1
USB_DP[0]	B6	I/O	Data Plus Bit 0
USB_DM[0]	C6	I/O	Data Minus Bit 0
USB_DM[1]	D7	I/O	Data Minus Bit 1
USB_PWR	W1	O	USB port power On/Off 0 = Power on 1 = Power off
USB_OVRCUR	W2	I	Indicates over current being drawn by a USB device 0 = Over current detected 1 = No over current

Table 9: IEEE 1394 port

Symbol	Pin	Type	Description
PHY_D[7]	B9	I/O	PHY Data Bit 7. Data is expected on pins 7:0 for 400 MB packets.
PHY_D[6]	D10	I/O	PHY Data Bit 6. Data is expected on pins 7:0 for 400 MB packets.
PHY_D[5]	C9	I/O	PHY Data Bit 5. Data is expected on pins 7:0 for 400 MB packets.
PHY_D[4]	A8	I/O	PHY Data Bit 4. Data is expected on pins 7:0 for 400 MB packets.
PHY_D[3]	B8	I/O	PHY Data Bit 3. Data is expected on pins 3:0 for 200 MB packets.
PHY_D[2]	D9	I/O	PHY Data Bit 2. Data is expected on pins 3:0 for 200 MB packets.
PHY_D[1]	C8	I/O	PHY Data Bit 1. Data is expected on pins 1:0 for 100 MB packets.
PHY_D[0]	A7	I/O	PHY Data Bit 0. Data is expected on pins 1:0 for 100 MB packets.
PHY_CTL[1]	B7	I/O	PHY Control Bit 1. Indicates the mode for data on the Din port.
PHY_CTL[0]	C7	I/O	PHY Control Bit 0. Indicates the mode for data on the Din port.
PHY_LREQ	B5	O	Used by the link to make bus requests and to access PHY registers. This is a serial bus. A train of pulses is sent on this signal.
PHY_ISO_N	A6	I	Signals which type of isolation mode is used at the PHY-Link interface. 0 = This is 1394-1995 Annex J type isolation. Enables differentiator circuitry. 1 = Direct connection or single capacitor isolation mode. This will disable the differentiator circuitry.
CLK_L1394	D8	I	System clock. 49.152 MHz input

Table 10: Serial communication port (I²C)

Symbol	Pin	Type	Description
I2C1_SCL	D6	I/O	Serial Communications Port (I ² C-bus) Clock
I2C1_SDA	A4	I/O	Serial Communications Port (I ² C-bus) Data
I2C2_SCL	H1	I/O	Serial Communications Port (I ² C-bus) Clock
I2C2_SDA	K4	I/O	Serial Communications Port (I ² C-bus) Data

Table 11: Audio and video interface

indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
DV_OUT1[9]	M2	O	Digital Video Output1, Bit 9 for primary display channel from AICP	
DV_OUT1[8]	M1	O	Digital Video Output1, Bit 8 for primary display channel from AICP	
DV_OUT1[7]	N4	O	Digital Video Output1, Bit 7 for primary display channel from AICP	
DV_OUT1[6]	N3	O	Digital Video Output1, Bit 6 for primary display channel from AICP	
DV_OUT1[5]	N1	O	Digital Video Output1, Bit 5 for primary display channel from AICP	
DV_OUT1[4]	N2	O	Digital Video Output1, Bit 4 for primary display channel from AICP	
DV_OUT1[3]	P2	O	Digital Video Output1, Bit 3 for primary display channel from AICP	
DV_OUT1[2]	P1	O	Digital Video Output1, Bit 2 for primary display channel from AICP	
DV_OUT1[1]	P4	O	Digital Video Output1, Bit 1 for primary display channel from AICP	
DV_OUT1[0]	P3	O	Digital Video Output1, Bit 0 for primary display channel from AICP	
DV_OUT2[9]	R2	O	Digital Video Output2, Bit 9 for secondary display channel from AICP	
DV_OUT2[8]	R4	O	Digital Video Output2, Bit 8 for secondary display channel from AICP	
DV_OUT2[7]	R3	O	Digital Video Output2, Bit 7 for secondary display channel from AICP	

Table 11: Audio and video interface...continued# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
DV_OUT2[6]	T1	O	Digital Video Output2, Bit 6 for secondary display channel from AICP	
DV_OUT2[5]	T2	O	Digital Video Output2, Bit 5 for secondary display channel from AICP	
DV_OUT2[4]	T3	O	Digital Video Output2, Bit 4 for secondary display channel from AICP	
DV_OUT2[3]	U1	O	Digital Video Output2, Bit 3 for secondary display channel from AICP	
DV_OUT2[2]	T4	O	Digital Video Output2, Bit 2 for secondary display channel from AICP	
DV_OUT2[1]	U2	O	Digital Video Output2, Bit 1 for secondary display channel from AICP	
DV_OUT2[0]	U3	O	Digital Video Output2, Bit 0 for secondary display channel from AICP	
DV_CLK1	M3	O	Digital Video Clock1 for primary display channel from AICP	
DV_CLK2	R1	O	Digital Video Clock2 for secondary display channel from AICP	
HSYNC	L1	O	Horizontal Sync for primary display	
VSYNC	L2	I/O	Vertical Sync for primary display	
BLANK	M4	O	Blanking for primary display	
I2S_IN1_OSCLK	AD20	O	Audio IN1 OverSample Clock	
I2S_IN1_SCK	AC19	I/O	Audio IN1 Serial Clock	
I2S_IN1_WS	AF21	I/O	Audio IN1 Word Select	
I2S_IN1_SD	AE21	I	Audio IN1 Data	
I2S_IN2_OSCLK	AD21	O	Audio IN2 OverSample Clock	
I2S_IN2_SCK	AC20	I/O	Audio IN2 Serial Clock	
I2S_IN2_WS	AF22	I/O	Audio IN2 Word Select	
I2S_IN2_SD	AE22	I	Audio IN2 Data	
I2S_IO_OSCLK	AF15	I/O	Audio IN/OUT OverSample Clock	#
I2S_IO_SCK	AE15	I/O	Audio IN/OUT Serial Clock	#
I2S_IO_WS	AC15	I/O	Audio IN/OUT Word Select	#
I2S_IO_SD[3]	AD15	I/O	Audio IN/OUT Data Bit 3	#
I2S_IO_SD[2]	AF16	I/O	Audio IN/OUT Data Bit 2	#
I2S_IO_SD[1]	AE16	I/O	Audio IN/OUT Data Bit 1	#
I2S_IO_SD[0]	AD16	I/O	Audio IN/OUT Data Bit 0	#
I2S_OUT1_OSCLK	K3	O	Audio OUT1 OverSample Clock	
I2S_OUT1_SCK	J1	I/O	Audio OUT1 Serial Clock	
I2S_OUT1_WS	J3	I/O	Audio OUT1 Word Select	
I2S_OUT1_SD	J2	O	Audio OUT1 Data	
I2S_OUT2_OSCLK	K2	O	Audio OUT2 OverSample Clock	#
I2S_OUT2_SCK	L3	I/O	Audio OUT2 Serial Clock	#
I2S_OUT2_WS	K1	I/O	Audio OUT2 Word Select	#
I2S_OUT2_SD	L4	O	Audio OUT2 Data	#
SPDIF_IN	AF17	I	Multi-ch/SPDIF Input	
SPDIF_OUT	AC16	O	Multi-ch/SPDIF Output	

Table 12: Digital video bus# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
DV1_DATA[9]	AE17	I/O	ITU-656 VIP Data Bit 9 (Most Significant Bit)	#
DV1_DATA[8]	AD17	I/O	ITU-656 VIP Data Bit 8	#
DV1_DATA[7]	AF18	I/O	ITU-656 VIP Data Bit 7	#
DV1_DATA[6]	AC17	I/O	ITU-656 VIP Data Bit 6	#
DV1_DATA[5]	AE18	I/O	ITU-656 VIP Data Bit 5	#
DV1_DATA[4]	AD18	I/O	ITU-656 VIP Data Bit 4	#
DV1_DATA[3]	AF19	I/O	ITU-656 VIP Data Bit 3	#
DV1_DATA[2]	AE19	I/O	ITU-656 VIP Data Bit 2	#
DV1_DATA[1]	AC18	I/O	ITU-656 VIP Data Bit 1	#
DV1_DATA[0]	AD19	I/O	ITU-656 VIP Data Bit 0 (Least Significant Bit)	#
DV1_VALID	AF20	I/O	ITU-656 VIP Data Valid	#
DV1_CLK	AE20	I/O	ITU-656 VIP Data Clock	#
DV2_DATA[7]	AF23	I	Digital Video Transport Stream2 Data Bit 7	#
DV2_DATA[6]	AC21	I	Digital Video Transport Stream2 Data Bit 6	#
DV2_DATA[5]	AD22	I	Digital Video Transport Stream2 Data Bit 5	#
DV2_DATA[4]	AE23	I	Digital Video Transport Stream2 Data Bit 4	#
DV2_DATA[3]	AC22	I	Digital Video Transport Stream2 Data Bit 3	#
DV2_DATA[2]	AD23	I	Digital Video Transport Stream2 Data Bit 2	#
DV2_DATA[1]	AE24	I	Digital Video Transport Stream2 Data Bit 1	#
DV2_DATA[0]	AF24	I	Digital Video Transport Stream2 Data Bit 0	#
DV2_SOP	AD24	I	Digital Video Transport Stream2 Start of Packet	#
DV2_ERR	AD26	I	Digital Video Transport Stream2 Error	#
DV2_VALID	AD25	I	Digital Video Transport Stream2 Data Valid	#
DV2_CLK	AC24	I	Digital Video Transport Stream2 Clock	#
DV3_DATA[7]	W23	I	Digital Video Transport Stream3 Data Bit 7	#
DV3_DATA[6]	Y24	I	Digital Video Transport Stream3 Data Bit 6	#
DV3_DATA[5]	Y25	I	Digital Video Transport Stream3 Data Bit 5	#
DV3_DATA[4]	Y26	I	Digital Video Transport Stream3 Data Bit 4	#
DV3_DATA[3]	W24	I	Digital Video Transport Stream3 Data Bit 3	#
DV3_DATA[2]	V23	I	Digital Video Transport Stream3 Data Bit 2	#
DV3_DATA[1]	W25	I	Digital Video Transport Stream3 Data Bit 1	#
DV3_DATA[0]	W26	I	Digital Video Transport Stream3 Data Bit 0	#
DV3_SOP	V24	I	Digital Video Transport Stream3 Start of Packet	#
DV3_ERR	U23	I	Digital Video Transport Stream3 Error	#
DV3_VALID	V25	I	Digital Video Transport Stream3 Data Valid	#
DV3_CLK	V26	I	Digital Video Transport Stream3 Clock	#
TS_DATA[7]	AB23	I/O	Transport Stream Data Bit 7	#
TS_DATA[6]	AC25	I/O	Transport Stream Data Bit 6	#
TS_DATA[5]	AB24	I/O	Transport Stream Data Bit 5	#

Table 12: Digital video bus...continued# indicates multiplexed signal, see [Section 6.2.1](#) for more details.

Symbol	Pin	Type	Description	Alternate Function
TS_DATA[4]	AA23	I/O	Transport Stream Data Bit 4	#
TS_DATA[3]	AC26	I/O	Transport Stream Data Bit 3	#
TS_DATA[2]	AB25	I/O	Transport Stream Data Bit 2	#
TS_DATA[1]	AB26	I/O	Transport Stream Data Bit 1	#
TS_DATA[0]	Y23	I/O	Transport Stream Data Bit 0	#
TS_SOP	AA24	I/O	Transport Stream Start of Packet (Parallel/Serial)	#
TS_VALID	AA25	I/O	Transport Stream Data Valid (Parallel/Serial)	#
TS_CLK	AA26	I/O	Transport Stream Clock (Parallel/Serial)	#

Table 13: Phase Lock Loop (PLL)

Symbol	Pin	Type	Description
XTALI	C2	I	PLL Reference Crystal Input
XTALO	D3	O	PLL Reference Crystal Feedback Driver
PLL_OUT	W4	O	General Purpose PLL Clock Output

Table 14: Analog and digital power (PWR)

Symbol	Pin	Description
V _D DC1	AB18	System 1.26 Volts
V _D DC1	AB17	System 1.26 Volts
V _D DC1	AB14	System 1.26 Volts
V _D DC1	AB13	System 1.26 Volts
V _D DC1	AB12	System 1.26 Volts
V _D DC1	AB9	System 1.26 Volts
V _D DC1	AB8	System 1.26 Volts
V _D DC1	N5	System 1.26 Volts
V _D DC1	P5	System 1.26 Volts
V _D DC1	U5	System 1.26 Volts
V _D DC1	V5	System 1.26 Volts
V _D DC1	K5	System 1.26 Volts
V _D DC1	J5	System 1.26 Volts
V _D DC1	E14	System 1.26 Volts
V _D DC1	E13	System 1.26 Volts
V _D DC1	E10	System 1.26 Volts
V _D DC1	E9	System 1.26 Volts
V _D DC1	E15	System 1.26 Volts
V _D DC1	E18	System 1.26 Volts
V _D DC1	E19	System 1.26 Volts
V _D DC1	U22	System 1.26 Volts
V _D DC1	V22	System 1.26 Volts
V _D DC1	P22	System 1.26 Volts

Table 14: Analog and digital power (PWR)...continued

Symbol	Pin	Description
V _{DDC1}	N22	System 1.26 Volts
V _{DDC1}	K22	System 1.26 Volts
V _{DDC1}	J22	System 1.26 Volts
V _{DDC1}	D1	System 1.26 Volts
V _{DDC1}	E2	System 1.26 Volts
V _{DDC1}	E1	System 1.26 Volts
V _{DDC1}	G4	System 1.26 Volts
V _{DDC1}	F3	System 1.26 Volts
V _{DDC1}	F2	System 1.26 Volts
V _{DDC1}	F1	System 1.26 Volts
V _{DDC1}	H4	System 1.26 Volts
V _{DDC1}	G3	System 1.26 Volts
V _{DDC2}	E4	System 1.26 Volts (Analog Power 1.728 GHz PLL)
V _{DDC2}	E3	System 1.26 Volts (Analog Power 1.728 GHz PLL)
V _{SS}	D2	System Ground (Analog Ground 1.728 GHz PLL)
V _{SS}	F4	System Ground (Analog Ground 1.728 GHz PLL)
V _{DD1}	AB6	System 3.3 Volts
V _{DD1}	AB7	System 3.3 Volts
V _{DD1}	AB10	System 3.3 Volts
V _{DD1}	AB11	System 3.3 Volts
V _{DD1}	AB16	System 3.3 Volts
V _{DD1}	AB19	System 3.3 Volts
V _{DD1}	AB20	System 3.3 Volts
V _{DD1}	E12	System 3.3 Volts
V _{DD1}	E11	System 3.3 Volts
V _{DD1}	E8	System 3.3 Volts
V _{DD1}	E7	System 3.3 Volts
V _{DD1}	E16	System 3.3 Volts
V _{DD1}	E17	System 3.3 Volts
V _{DD1}	E20	System 3.3 Volts
V _{DD1}	E21	System 3.3 Volts
V _{DD1}	M22	System 3.3 Volts
V _{DD1}	L22	System 3.3 Volts
V _{DD1}	H22	System 3.3 Volts
V _{DD1}	G22	System 3.3 Volts
V _{DD1}	R22	System 3.3 Volts
V _{DD1}	T22	System 3.3 Volts
V _{DD1}	W22	System 3.3 Volts
V _{DD1}	Y22	System 3.3 Volts
V _{DD1}	T5	System 3.3 Volts
V _{DD1}	R5	System 3.3 Volts

Table 14: Analog and digital power (PWR)...continued

Symbol	Pin	Description
V _{DD1}	M5	System 3.3 Volts
V _{DD1}	L5	System 3.3 Volts
V _{DD1}	W5	System 3.3 Volts
V _{DD1}	Y5	System 3.3 Volts
V _{DD2}	G5	System 3.3 Volts (CAB)
V _{DD2}	H5	System 3.3 Volts (CAB)
V _{DD3}	AB15	System 3.3 Volts (TM-PLL)
V _{SS}	AF25	System Ground
V _{SS}	AF26	System Ground
V _{SS}	AE26	System Ground
V _{SS}	AE25	System Ground
V _{SS}	AC23	System Ground
V _{SS}	AB22	System Ground
V _{SS}	AB21	System Ground
V _{SS}	AA22	System Ground
V _{SS}	F22	System Ground
V _{SS}	E22	System Ground
V _{SS}	D23	System Ground
V _{SS}	C24	System Ground
V _{SS}	B25	System Ground
V _{SS}	A25	System Ground
V _{SS}	A26	System Ground
V _{SS}	B26	System Ground
V _{SS}	L15	System Ground
V _{SS}	L14	System Ground
V _{SS}	L13	System Ground
V _{SS}	L12	System Ground
V _{SS}	L11	System Ground
V _{SS}	M11	System Ground
V _{SS}	N11	System Ground
V _{SS}	P11	System Ground
V _{SS}	R11	System Ground
V _{SS}	T11	System Ground
V _{SS}	T12	System Ground
V _{SS}	T13	System Ground
V _{SS}	R13	System Ground
V _{SS}	R14	System Ground
V _{SS}	T14	System Ground
V _{SS}	T15	System Ground
V _{SS}	T16	System Ground
V _{SS}	R16	System Ground

Table 14: Analog and digital power (PWR)...continued

Symbol	Pin	Description
V _{SS}	AA5	System Ground
V _{SS}	AB5	System Ground
V _{SS}	AC4	System Ground
V _{SS}	AD3	System Ground
V _{SS}	AE2	System Ground
V _{SS}	AE1	System Ground
V _{SS}	AF1	System Ground
V _{SS}	AF2	System Ground
V _{SS}	F5	System Ground
V _{SS}	E5	System Ground
V _{SS}	E6	System Ground
V _{SS}	D4	System Ground
V _{SS}	B2	System Ground
V _{SS}	A2	System Ground
V _{SS}	A1	System Ground
V _{SS}	B1	System Ground
V _{SS}	R15	System Ground
V _{SS}	R12	System Ground
V _{SS}	P12	System Ground
V _{SS}	P13	System Ground
V _{SS}	N13	System Ground
V _{SS}	N14	System Ground
V _{SS}	P14	System Ground
V _{SS}	P15	System Ground
V _{SS}	P16	System Ground
V _{SS}	N16	System Ground
V _{SS}	N15	System Ground
V _{SS}	N12	System Ground
V _{SS}	M12	System Ground
V _{SS}	M13	System Ground
V _{SS}	M14	System Ground
V _{SS}	L16	System Ground
V _{SS}	M16	System Ground
V _{SS}	M15	System Ground

Table 15: Test

Symbol	Pin	Type	Description
DBG_TDI	A3	I	PR3940 Debug Port Data In
DBG_TDO	B3	O	PR3940 Debug Port Data Out
DBG_TCK	C3	I	PR3940 Debug Port Clock
DBG_TMS	C1	I	PR3940 Debug Port Mode Select

Table 15: Test...continued

Symbol	Pin	Type	Description
JTAG_TRST	G2	I	JTAG Port Reset
JTAG_TDI	J4	I	JTAG Data IN
JTAG_TDO	H2	O	JTAG Data OUT
JTAG_TCK	G1	I	JTAG Data Clock
JTAG_TMS	H3	I	JTAG Data Mode Select

Table 16: All pins

Symbol	Pin	Group	Type	Description
V _{SS}	A1	PWR	-	System Ground
V _{SS}	A2	PWR	-	System Ground
DBG_TDI	A3	TEST	I	PR3940 Debug Port Data In
I2C_SDA	A4	I ² C-bus	I/O	Serial Communications Port (I ² C-bus) Data
USB_DP[1]	A5	USB	I/O	Data Plus Bit 1
PHY_ISO_N	A6	1394	I	Signals type of isolation mode used at the PHY-Link interface. 0 = 1394-1995 Annex J type isolation. Enables differentiator circuitry. 1 = Direct connection or single capacitor isolation mode. This will disable the differentiator circuitry.
PHY_D[0]	A7	1394	I/O	PHY Data Bit 0. Data is expected on pins 1:0 for 100 MB packets.
PHY_D[4]	A8	1394	I/O	PHY Data Bit 4. Data is expected on pins 7:0 for 400 MB packets.
MDQM[0]	A9	MMI	O	SDRAM Control Bit 0
MD[03]	A10	MMI	I/O	Memory Data Bit 03
MD[06]	A11	MMI	I/O	Memory Data Bit 06
MD[09]	A12	MMI	I/O	Memory Data Bit 09
MD[13]	A13	MMI	I/O	Memory Data Bit 13
MD[15]	A14	MMI	I/O	Memory Data Bit 15
MD[20]	A15	MMI	I/O	Memory Data Bit 20
MD[24]	A16	MMI	I/O	Memory Data Bit 24
MDQM[3]	A17	MMI	O	SDRAM Control Bit 3
MD[31]	A18	MMI	I/O	Memory Data Bit 31
MD[28]	A19	MMI	I/O	Memory Data Bit 28
MA[7]	A20	MMI	O	Memory Address Bit 7
MA[9]	A21	MMI	O	Memory Address Bit 9
MCS	A22	MMI	O	Memory Chip Select
MCAS	A23	MMI	O	Memory Column Address Select
MDQM[4]	A24	MMI	O	SDRAM Control Bit 4
V _{SS}	A25	PWR	-	System Ground
V _{SS}	A26	PWR	-	System Ground
V _{SS}	B1	PWR	-	System Ground
V _{SS}	B2	PWR	-	System Ground
DBG_TDO	B3	TEST	O	PR3940 Debug Port Data Out
GPIO[2]	B4	GPIO	I/O	General Purpose Input/Output Bit 2

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
PHY_LREQ	B5	1394	O	Used by the link to make bus requests and to access PHY registers. This is a serial bus. A train of pulses is sent on this signal.
USB_DP[0]	B6	USB	I/O	Data Plus Bit 0
PHY_CTL[1]	B7	1394	I/O	PHY Control Bit 1. Indicates the mode for data on the Din port.
PHY_D[3]	B8	1394	I/O	PHY Data Bit 3. Data is expected on pins 3:0 for 200 MB packets.
PHY_D[7]	B9	1394	I/O	PHY Data Bit 7. Data is expected on pins 7:0 for 400 MB packets.
MD[01]	B10	MMI	I/O	Memory Data Bit 01
MD[05]	B11	MMI	I/O	Memory Data Bit 05
MD[08]	B12	MMI	I/O	Memory Data Bit 08
MD[12]	B13	MMI	I/O	Memory Data Bit 12
MDQM[2]	B14	MMI	O	SDRAM Control Bit 2
MD[19]	B15	MMI	I/O	Memory Data Bit 19
MD[23]	B16	MMI	I/O	Memory Data Bit 23
MD[27]	B17	MMI	I/O	Memory Data Bit 27
MD[30]	B18	MMI	I/O	Memory Data Bit 30
MCLK[0]	B19	MMI	O	Memory Clock
MA[1]	B20	MMI	O	Memory Address Bit 1
MA[10]	B21	MMI	O	Memory Address Bit 10
MBA[0]	B22	MMI	O	SDRAM Bank Select
MRAS	B23	MMI	O	EDODRAM Row Address Strobe
MWE	B24	MMI	O	Memory Write Enable
V _{SS}	B25	PWR	-	System Ground
V _{SS}	B26	PWR	-	System Ground
DBG_TMS	C1	TEST	I	PR3940 Debug Port Mode Select
XTALI	C2	PLL	I	PLL Reference Crystal Input
DBG_TCK	C3	TEST	I	PR3940 Debug Port Clock
GPIO[0]	C4	GPIO	I/O	General Purpose Input/Output Bit 0
GPIO[3]	C5	GPIO	I/O	General Purpose Input/Output Bit 3
USB_DM[0]	C6	USB	I/O	Data Minus Bit 0
PHY_CTL[0]	C7	1394	I/O	PHY Control Bit 0. Indicates the mode for data on the Din port.
PHY_D[1]	C8	1394	I/O	PHY Data Bit 1. Data is expected on pins 1:0 for 100 MB packets.
PHY_D[5]	C9	1394	I/O	PHY Data Bit 5. Data is expected on pins 7:0 for 400 MB packets.
MD[00]	C10	MMI	I/O	Memory Data Bit 00
MD[02]	C11	MMI	I/O	Memory Data Bit 02
MD[07]	C12	MMI	I/O	Memory Data Bit 07
MD[11]	C13	MMI	I/O	Memory Data Bit 11
MD[16]	C14	MMI	I/O	Memory Data Bit 16
MD[18]	C15	MMI	I/O	Memory Data Bit 18
MD[22]	C16	MMI	I/O	Memory Data Bit 22
MD[26]	C17	MMI	I/O	Memory Data Bit 26
MD[29]	C18	MMI	I/O	Memory Data Bit 29

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
MA[3]	C19	MMI	O	Memory Address Bit 3
MA[6]	C20	MMI	O	Memory Address Bit 6
MA[8]	C21	MMI	O	Memory Address Bit 8
MA[11]	C22	MMI	O	Memory Address Bit 11
MCKE	C23	MMI	O	Memory Clock Enable
V _{SS}	C24	PWR	-	System Ground
MD[32]	C25	MMI	I/O	Memory Data Bit 32
MCLK[1]	C26	MMI	O	Memory Clock
V _{DDC}	D1	PWR	-	System 1.26 Volts
V _{SS}	D2	PWR	-	System Ground (Analog Ground 1.728 GHz PLL)
XTALO	D3	PLL	O	PLL Reference Crystal Feedback Driver
V _{SS}	D4	PWR	-	System Ground
GPIO[1]	D5	GPIO	I/O	General Purpose Input/Output Bit 1
I2C_SCL	D6	I ² C-bus	I/O	Serial Communications Port (I ² C-bus) Clock
USB_DM[1]	D7	USB	I/O	Data Minus Bit 1
CLK_L1394	D8	1394	I	System clock. 49.152 MHz input
PHY_D[2]	D9	1394	I/O	PHY Data Bit 2. Data is expected on pins 3:0 for 200 MB packets.
PHY_D[6]	D10	1394	I/O	PHY Data Bit 6. Data is expected on pins 7:0 for 400 MB packets.
MD[04]	D11	MMI	I/O	Memory Data Bit 04
MDQM[1]	D12	MMI	O	SDRAM Control Bit 1
MD[10]	D13	MMI	I/O	Memory Data Bit 10
MD[14]	D14	MMI	I/O	Memory Data Bit 14
MD[17]	D15	MMI	I/O	Memory Data Bit 17
MD[21]	D16	MMI	I/O	Memory Data Bit 21
MD[25]	D17	MMI	I/O	Memory Data Bit 25
MA[5]	D18	MMI	O	Memory Address Bit 5
MA[4]	D19	MMI	O	Memory Address Bit 4
MA[2]	D20	MMI	O	Memory Address Bit 2
MA[0]	D21	MMI	O	Memory Address Bit 0
MBA[1]	D22	MMI	O	SDRAM Bank Select
V _{SS}	D23	PWR	-	System Ground
MD[33]	D24	MMI	I/O	Memory Data Bit 33
MD[36]	D25	MMI	I/O	Memory Data Bit 36
MD[35]	D26	MMI	I/O	Memory Data Bit 35
V _{DDC1}	E1	PWR	-	System 1.26 Volts
V _{DDC1}	E2	PWR	-	System 1.26 Volts
V _{DDC2}	E3	PWR	-	System 1.26 Volts (Analog Power 1.728 GHz PLL)
V _{DDC2}	E4	PWR	-	System 1.26 Volts (Analog Power 1.728 GHz PLL)
V _{SS}	E5	PWR	-	System Ground
V _{SS}	E6	PWR	-	System Ground
V _{DD1}	E7	PWR	-	System 3.3 Volts

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
V _{DD1}	E8	PWR	-	System 3.3 Volts
V _{DDC1}	E9	PWR	-	System 1.26 Volts
V _{DDC1}	E10	PWR	-	System 1.26 Volts
V _{DD1}	E11	PWR	-	System 3.3 Volts
V _{DD1}	E12	PWR	-	System 3.3 Volts
V _{DDC1}	E13	PWR	-	System 1.26 Volts
V _{DDC1}	E14	PWR	-	System 1.26 Volts
V _{DDC1}	E15	PWR	-	System 1.26 Volts
V _{DD1}	E16	PWR	-	System 3.3 Volts
V _{DD1}	E17	PWR	-	System 3.3 Volts
V _{DDC1}	E18	PWR	-	System 1.26 Volts
V _{DDC1}	E19	PWR	-	System 1.26 Volts
V _{DD1}	E20	PWR	-	System 3.3 Volts
V _{DD1}	E21	PWR	-	System 3.3 Volts
V _{SS}	E22	PWR	-	System Ground
MD[34]	E23	MMI	I/O	Memory Data Bit 34
MD[37]	E24	MMI	I/O	Memory Data Bit 37
MD[38]	E25	MMI	I/O	Memory Data Bit 38
MDQM[5]	E26	MMI	O	SDRAM Control Bit 5
V _{DDC1}	F1	PWR	-	System 1.26 Volts
V _{DDC1}	F2	PWR	-	System 1.26 Volts
V _{DDC1}	F3	PWR	-	System 1.26 Volts
V _{SS}	F4	PWR	-	System Ground (Analog Ground 1.728 GHz PLL)
V _{SS}	F5	PWR	-	System Ground
V _{SS}	F22	PWR	-	System Ground
MD[39]	F23	MMI	I/O	Memory Data Bit 39
MD[40]	F24	MMI	I/O	Memory Data Bit 40
MD[41]	F25	MMI	I/O	Memory Data Bit 41
MD[42]	F26	MMI	I/O	Memory Data Bit 42
JTAG_TCK	G1	TEST	I	JTAG Data Clock
JTAG_TRST	G2	TEST	I	JTAG Port Reset
V _{DDC1}	G3	PWR	-	System 1.26 Volts
V _{DDC1}	G4	PWR	-	System 1.26 Volts
V _{DD2}	G5	PWR	-	System 3.3 Volts (CAB)
V _{DD1}	G22	PWR	-	System 3.3 Volts
MD[43]	G23	MMI	I/O	Memory Data Bit 43
MD[44]	G24	MMI	I/O	Memory Data Bit 44
MD[45]	G25	MMI	I/O	Memory Data Bit 45
MD[46]	G26	MMI	I/O	Memory Data Bit 46
I2C2_SCL	H1	I ² C-bus	I/O	Serial Communications Port (I ² C-bus) Clock
JTAG_TDO	H2	TEST	O	JTAG Data OUT

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
JTAG_TMS	H3	TEST	I	JTAG Data Mode Select
V _{DDC1}	H4	PWR	-	System 1.26 Volts
V _{DD2}	H5	PWR	-	System 3.3 Volts (CAB)
V _{DD1}	H22	PWR	-	System 3.3 Volts
MD[47]	H23	MMI	I/O	Memory Data Bit 47
MDQM[6]	H24	MMI	O	SDRAM Control Bit 6
MD[48]	H25	MMI	I/O	Memory Data Bit 48
MD[49]	H26	MMI	I/O	Memory Data Bit 49
I2S_OUT1_SCK	J1	AVIF	I/O	Audio OUT1 Serial Clock
I2S_OUT1_SD	J2	AVIF	O	Audio OUT1 Data
I2S_OUT1_WS	J3	AVIF	I/O	Audio OUT1 Word Select
JTAG_TDI	J4	TEST	I	JTAG Data IN
V _{DDC1}	J5	PWR	-	System 1.26 Volts
V _{DDC1}	J22	PWR	-	System 1.26 Volts
MD[50]	J23	MMI	I/O	Memory Data Bit 50
MD[51]	J24	MMI	I/O	Memory Data Bit 51
MD[52]	J25	MMI	I/O	Memory Data Bit 52
MD[53]	J26	MMI	I/O	Memory Data Bit 53
I2S_OUT2_WS	K1	AVIF	I/O	Audio OUT2 Word Select
I2S_OUT2_OSCLK	K2	AVIF	O	Audio OUT2 OverSample Clock
I2S_OUT1_OSCLK	K3	AVIF	O	Audio OUT1 OverSample Clock
I2C2_SDA	K4	I ² C-bus	I/O	Serial Communications Port (I ² C-bus) Data
V _{DDC1}	K5	PWR	-	System 1.26 Volts
V _{DDC1}	K22	PWR	-	System 1.26 Volts
MD[54]	K23	MMI	I/O	Memory Data Bit 54
MD[55]	K24	MMI	I/O	Memory Data Bit 55
MDQM[7]	K25	MMI	O	SDRAM Control Bit 7
MD[56]	K26	MMI	I/O	Memory Data Bit 56
HSYNC	L1	AVIF	O	Horizontal Sync for primary display
VSYN	L2	AVIF	I/O	Vertical Sync for primary display
I2S_OUT2_SCK	L3	AVIF	I/O	Audio OUT2 Serial Clock
I2S_OUT2_SD	L4	AVIF	O	Audio OUT2 Data
V _{DD1}	L5	PWR	-	System 3.3 Volts
V _{SS}	L11	PWR	-	System Ground
V _{SS}	L12	PWR	-	System Ground
V _{SS}	L13	PWR	-	System Ground
V _{SS}	L14	PWR	-	System Ground
V _{SS}	L15	PWR	-	System Ground
V _{SS}	L16	PWR	-	System Ground
V _{DD1}	L22	PWR	-	System 3.3 Volts
MD[57]	L23	MMI	I/O	Memory Data Bit 57

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
MD[58]	L24	MMI	I/O	Memory Data Bit 58
MD[59]	L25	MMI	I/O	Memory Data Bit 59
MD[60]	L26	MMI	I/O	Memory Data Bit 60
DV_OUT1[8]	M1	AVIF	O	Digital Video Output1, Bit 8 for primary display channel from AICP
DV_OUT1[9]	M2	AVIF	O	Digital Video Output1, Bit 9 for primary display channel from AICP
DV_CLK1	M3	AVIF	O	Digital Video Clock1 for primary display channel from AICP
BLANK	M4	AVIF	O	Blanking for primary display
V _{DD1}	M5	PWR	-	System 3.3 Volts
V _{SS}	M11	PWR	-	System Ground
V _{SS}	M12	PWR	-	System Ground
V _{SS}	M13	PWR	-	System Ground
V _{SS}	M14	PWR	-	System Ground
V _{SS}	M15	PWR	-	System Ground
V _{SS}	M16	PWR	-	System Ground
V _{DD1}	M22	PWR	-	System 3.3 Volts
MD[61]	M23	MMI	I/O	Memory Data Bit 61
MD[62]	M24	MMI	I/O	Memory Data Bit 62
MD[63]	M25	MMI	I/O	Memory Data Bit 63
GPIO[8]	M26	GPIO	I/O	General Purpose Input/Output Bit 8
DV_OUT1[5]	N1	AVIF	O	Digital Video Output1, Bit 5 for primary display channel from AICP
DV_OUT1[4]	N2	AVIF	O	Digital Video Output1, Bit 4 for primary display channel from AICP
DV_OUT1[6]	N3	AVIF	O	Digital Video Output1, Bit 6 for primary display channel from AICP
DV_OUT1[7]	N4	AVIF	O	Digital Video Output1, Bit 7 for primary display channel from AICP
V _{DDC1}	N5	PWR	-	System 1.26 Volts
V _{SS}	N11	PWR	-	System Ground
V _{SS}	N12	PWR	-	System Ground
V _{SS}	N13	PWR	-	System Ground
V _{SS}	N14	PWR	-	System Ground
V _{SS}	N15	PWR	-	System Ground
V _{SS}	N16	PWR	-	System Ground
V _{DDC1}	N22	PWR	-	System 1.26 Volts
GPIO[9]	N23	GPIO	I/O	General Purpose Input/Output Bit 9
GPIO[10]	N24	GPIO	I/O	General Purpose Input/Output Bit 10
SC2_SCCK	N25	COM	O	Smart Card2 Bit Clock
GPIO[11]	N26	GPIO	I/O	General Purpose Input/Output Bit 11
DV_OUT1[2]	P1	AVIF	O	Digital Video Output1, Bit 2 for primary display channel from AICP
DV_OUT1[3]	P2	AVIF	O	Digital Video Output1, Bit 3 for primary display channel from AICP
DV_OUT1[0]	P3	AVIF	O	Digital Video Output1, Bit 0 for primary display channel from AICP
DV_OUT1[1]	P4	AVIF	O	Digital Video Output1, Bit 1 for primary display channel from AICP
V _{DDC1}	P5	PWR	-	System 1.26 Volts
V _{SS}	P11	PWR	-	System Ground

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
V _{SS}	P12	PWR	-	System Ground
V _{SS}	P13	PWR	-	System Ground
V _{SS}	P14	PWR	-	System Ground
V _{SS}	P15	PWR	-	System Ground
V _{SS}	P16	PWR	-	System Ground
V _{DDC1}	P22	PWR	-	System 1.26 Volts
SC2_DA	P23	COM	I/O	Smart Card2 Data
SC2_CMD	P24	COM	O	Smart Card2 Command
SC2_OFFN	P25	COM	I	Smart Card2 Off
SC2_RST	P26	COM	O	Smart Card2 Reset
DV_CLK2	R1	AVIF	O	Digital Video Clock2 for secondary display channel from AICP
DV_OUT2[9]	R2	AVIF	O	Digital Video Output2, Bit 9 for secondary display channel from AICP
DV_OUT2[7]	R3	AVIF	O	Digital Video Output2, Bit 7 for secondary display channel from AICP
DV_OUT2[8]	R4	AVIF	O	Digital Video Output2, Bit 8 for secondary display channel from AICP
V _{DD1}	R5	PWR	-	System 3.3 Volts
V _{SS}	R11	PWR	-	System Ground
V _{SS}	R12	PWR	-	System Ground
V _{SS}	R13	PWR	-	System Ground
V _{SS}	R14	PWR	-	System Ground
V _{SS}	R15	PWR	-	System Ground
V _{SS}	R16	PWR	-	System Ground
V _{DD1}	R22	PWR	-	System 3.3 Volts
SC1_CMD	R23	COM	O	Smart Card1 Command
SC1_RST	R24	COM	O	Smart Card1 Reset
SC1_OFFN	R25	COM	I	Smart Card1 Off
SC1_SCCK	R26	COM	O	Smart Card1 Bit Clock
DV_OUT2[6]	T1	AVIF	O	Digital Video Output2, Bit 6 for secondary display channel from AICP
DV_OUT2[5]	T2	AVIF	O	Digital Video Output2, Bit 5 for secondary display channel from AICP
DV_OUT2[4]	T3	AVIF	O	Digital Video Output2, Bit 4 for secondary display channel from AICP
DV_OUT2[2]	T4	AVIF	O	Digital Video Output2, Bit 2 for secondary display channel from AICP
V _{DD1}	T5	PWR	-	System 3.3 Volts
V _{SS}	T11	PWR	-	System Ground
V _{SS}	T12	PWR	-	System Ground
V _{SS}	T13	PWR	-	System Ground
V _{SS}	T14	PWR	-	System Ground
V _{SS}	T15	PWR	-	System Ground
V _{SS}	T16	PWR	-	System Ground
V _{DD1}	T22	PWR	-	System 3.3 Volts
UA2_TX	T23	COM	I/O	UART2 Transmit
UA2_RTSEN	T24	COM	I/O	UART2 Request To Send
UA2_CTSEN	T25	COM	I/O	UART2 Clear To Send

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
SC1_DA	T26	COM	I/O	Smart Card1 Data
DV_OUT2[3]	U1	AVIF	O	Digital Video Output2, Bit 3 for secondary display channel from AICP
DV_OUT2[1]	U2	AVIF	O	Digital Video Output2, Bit 1 for secondary display channel from AICP
DV_OUT2[0]	U3	AVIF	O	Digital Video Output2, Bit 0 for secondary display channel from AICP
SSI_RXD	U4	COM	I/O	Synchronous Serial Interface Receive
V _{DDC1}	U5	PWR	-	System 1.26 Volts
V _{DDC1}	U22	PWR	-	System 1.26 Volts
DV3_ERR	U23	DVB	I	Digital Video Transport Stream3 Error
UA1_TX	U24	COM	I/O	UART1 Transmit
UA1_RX	U25	COM	I/O	UART1 Receive
UA2_RX	U26	COM	I/O	UART2 Receive
SSI_SCLK_CTSN	V1	COM	I/O	Synchronous Serial Interface CLock
SSI_FS_RTSN	V2	COM	I/O	Synchronous Serial Interface Frame Sync
SSI_TXD	V3	COM	I/O	Synchronous Serial Interface Transmit
INTA	V4	PCI	I/O	Interrupt Acknowledge is asserted to request an interrupt.
V _{DDC1}	V5	PWR	-	System 1.26 Volts
V _{DDC1}	V22	PWR	-	System 1.26 Volts
DV3_DATA[2]	V23	DVB	I	Digital Video Transport Stream3 Data Bit 2
DV3_SOP	V24	DVB	I	Digital Video Transport Stream3 Start of Packet
DV3_VALID	V25	DVB	I	Digital Video Transport Stream3 Data Valid
DV3_CLK	V26	DVB	I	Digital Video Transport Stream3 Clock
USB_PWR	W1	USB	O	USB port power On/Off 0 = Power on 1 = Power off
USB_OVRCUR	W2	USB	I	Indicates over current being drawn by a USB device: 0 = Over current detected 1 = No over current
RESET_IN	W3	PCI	I	PCI Bus Global Reset
PLL_OUT	W4	PLL	O	General Purpose PLL Clock Output
V _{DD1}	W5	PWR	-	System 3.3 Volts
V _{DD1}	W22	PWR	-	System 3.3 Volts
DV3_DATA[7]	W23	DVB	I	Digital Video Transport Stream3 Data Bit 7
DV3_DATA[3]	W24	DVB	I	Digital Video Transport Stream3 Data Bit 3
DV3_DATA[1]	W25	DVB	I	Digital Video Transport Stream3 Data Bit 1
DV3_DATA[0]	W26	DVB	I	Digital Video Transport Stream3 Data Bit 0
SYS_RSTN_OUT	Y1	MISC	O	System Reset Output
REQ	Y2	PCI	I/O	Arbitration Request on PCI Bus. Request is an output when using an external arbiter and an input when using an internal arbiter.
GNT	Y3	PCI	I/O	Arbitration Grant is asserted to indicate access to the bus has been granted. This pin is an input when an external arbiter is used and an output when using the internal arbiter.

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
GNT_A	Y4	PCI	I/O	Auxiliary Arbitration Grant_A is asserted to indicate bus access has been granted to an external PCI master. Used where internal arbiter is configured.
V _{DD1}	Y5	PWR	-	System 3.3 Volts
V _{DD1}	Y22	PWR	-	System 3.3 Volts
TS_DATA[0]	Y23	DVB	I/O	Transport Stream Data Bit 0
DV3_DATA[6]	Y24	DVB	I	Digital Video Transport Stream3 Data Bit 6
DV3_DATA[5]	Y25	DVB	I	Digital Video Transport Stream3 Data Bit 5
DV3_DATA[4]	Y26	DVB	I	Digital Video Transport Stream3 Data Bit 4
CLK	AA1	PCI	I	PCI Bus Clock
REQ_A	AA2	PCI	I/O	Auxiliary Arbitration REQ_A on PCI Bus. Used in modes where internal arbiter is configured.
REQ_B	AA3	PCI	I/O	Auxiliary Arbitration REQ_B on PCI Bus. Used in modes where internal arbiter is configured.
GNT_B	AA4	PCI	I/O	Auxiliary Arbitration Grant_B is asserted to indicate bus access has been granted to an external PCI master. Used where internal arbiter is configured.
V _{SS}	AA5	PWR	-	System Ground
V _{SS}	AA22	PWR	-	System Ground
TS_DATA[4]	AA23	DVB	I/O	Transport Stream Data Bit 4
TS_SOP	AA24	DVB	I/O	Transport Stream Start of Packet (Parallel/Serial)
TS_VALID	AA25	DVB	I/O	Transport Stream Data Valid (Parallel/Serial)
TS_CLK	AA26	DVB	I/O	Transport Stream Clock (Parallel/Serial)
AD[31]	AB1	PCI	I/O	Multiplexed Address or Data Bit 31
AD[30]	AB2	PCI	I/O	Multiplexed Address or Data Bit 30
AD[29]	AB3	PCI	I/O	Multiplexed Address or Data Bit 29
AD[28]	AB4	PCI	I/O	Multiplexed Address or Data Bit 28
V _{SS}	AB5	PWR	-	System Ground
V _{DD1}	AB6	PWR	-	System 3.3 Volts
V _{DD1}	AB7	PWR	-	System 3.3 Volts
V _{DDC1}	AB8	PWR	-	System 1.26 Volts
V _{DDC1}	AB9	PWR	-	System 1.26 Volts
V _{DD1}	AB10	PWR	-	System 3.3 Volts
V _{DD1}	AB11	PWR	-	System 3.3 Volts
V _{DDC1}	AB12	PWR	-	System 1.26 Volts
V _{DDC1}	AB13	PWR	-	System 1.26 Volts
V _{DDC1}	AB14	PWR	-	System 1.26 Volts
V _{DD1}	AB15	PWR	-	System 3.3 Volts (TM-PLL)
V _{DD3}	AB16	PWR	-	System 3.3 Volts
V _{DDC1}	AB17	PWR	-	System 1.26 Volts
V _{DDC1}	AB18	PWR	-	System 1.26 Volts

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
V _{DD1}	AB19	PWR	-	System 3.3 Volts
V _{DD1}	AB20	PWR	-	System 3.3 Volts
V _{SS}	AB21	PWR	-	System Ground
V _{SS}	AB22	PWR	-	System Ground
TS_DATA[7]	AB23	DVB	I/O	Transport Stream Data Bit 7
TS_DATA[5]	AB24	DVB	I/O	Transport Stream Data Bit 5
TS_DATA[2]	AB25	DVB	I/O	Transport Stream Data Bit 2
TS_DATA[1]	AB26	DVB	I/O	Transport Stream Data Bit 1
AD[27]	AC1	PCI	I/O	Multiplexed Address or Data Bit 27
AD[26]	AC2	PCI	I/O	Multiplexed Address or Data Bit 26
AD[25]	AC3	PCI	I/O	Multiplexed Address or Data Bit 25
V _{SS}	AC4	PWR	-	System Ground
AD[17]	AC5	PCI	I/O	Multiplexed Address or Data Bit 17
AD[16]	AC6	PCI	I/O	Multiplexed Address or Data Bit 16
SERR	AC7	PCI	I/O	System Error
AD[14]	AC8	PCI	I/O	Multiplexed Address or Data Bit 14
AD[10]	AC9	PCI	I/O	Multiplexed Address or Data Bit 10
AD[07]	AC10	PCI	I/O	Multiplexed Address or Data Bit 7
AD[03]	AC11	PCI	I/O	Multiplexed Address or Data Bit 3
AD[00]	AC12	PCI	I/O	Multiplexed Address or Data Bit 0
XIO_SEL[1]	AC13	MISC	I/O	External I/O Select1
GPIO[4]	AC14	GPIO	I/O	General Purpose Input/Output Bit 4
I2S_IO_WS	AC15	AVIF	I/O	Audio IN/OUT Word Select
SPDIF_OUT	AC16	AVIF	O	Multi-channel/SPDIF Output
DV1_DATA[6]	AC17	DVB	I/O	ITU-656 VIP Data Bit 6
DV1_DATA[1]	AC18	DVB	I/O	ITU-656 VIP Data Bit 1
I2S_IN1_SCK	AC19	AVIF	I/O	Audio IN1 Serial Clock
I2S_IN2_SCK	AC20	AVIF	I/O	Audio IN2 Serial Clock
DV2_DATA[6]	AC21	DVB	I	Digital Video Transport Stream2 Data Bit 6
DV2_DATA[3]	AC22	DVB	I	Digital Video Transport Stream2 Data Bit 3
V _{SS}	AC23	PWR	-	System Ground
DV2_CLK	AC24	DVB	I	Digital Video Transport Stream2 Clock
TS_DATA[6]	AC25	DVB	I/O	Transport Stream Data Bit 6
TS_DATA[3]	AC26	DVB	I/O	Transport Stream Data Bit 3
C/BE[3]	AD1	PCI	I/O	Multiplexed Command or Byte Enable 3
AD[24]	AD2	PCI	I/O	Multiplexed Address or Data Bit 24
V _{SS}	AD3	PWR	-	System Ground
AD[20]	AD4	PCI	I/O	Multiplexed Address or Data Bit 20
AD[18]	AD5	PCI	I/O	Multiplexed Address or Data Bit 18

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
TRDY	AD6	PCI	I/O	Parity Error indicates data parity errors during all PCI transactions except Special Cycle.
PERR	AD7	PCI	I/O	Parity Error indicates data parity errors during all PCI transactions except Special Cycle.
AD[15]	AD8	PCI	I/O	Multiplexed Address or Data Bit 15
AD[11]	AD9	PCI	I/O	Multiplexed Address or Data Bit 11
C/BE[0]	AD10	PCI	I/O	Multiplexed Command or Byte Enable 0
AD[04]	AD11	PCI	I/O	Multiplexed Address or Data Bit 4
AD[01]	AD12	PCI	I/O	Multiplexed Address or Data Bit 1
XIO_SEL[0]	AD13	MISC	I/O	External I/O Select0
GPIO[5]	AD14	GPIO	I/O	General Purpose Input/Output Bit 5
I2S_IO_SD[3]	AD15	AVIF	I/O	Audio IN/OUT Data Bit 3
I2S_IO_SD[0]	AD16	AVIF	I/O	Audio IN/OUT Data Bit 0
DV1_DATA[8]	AD17	DVB	I/O	ITU-656 VIP Data Bit 8
DV1_DATA[4]	AD18	DVB	I/O	ITU-656 VIP Data Bit 4
DV1_DATA[0]	AD19	DVB	I/O	ITU-656 VIP Data Bit 0 (Least Significant Bit)
I2S_IN1_OSCLK	AD20	AVIF	O	Audio IN1 OverSample Clock
I2S_IN2_OSCLK	AD21	AVIF	O	Audio IN2 OverSample Clock
DV2_DATA[5]	AD22	DVB	I	Digital Video Transport Stream2 Data Bit 5
DV2_DATA[2]	AD23	DVB	I	Digital Video Transport Stream2 Data Bit 2
DV2_SOP	AD24	DVB	I	Digital Video Transport Stream2 Start of Packet
DV2_VALID	AD25	DVB	I	Digital Video Transport Stream2 Data Valid
DV2_ERR	AD26	DVB	I	Digital Video Transport Stream2 Error
V _{SS}	AE1	PWR	-	System Ground
V _{SS}	AE2	PWR	-	System Ground
AD[23]	AE3	PCI	I/O	Multiplexed Address or Data Bit 23
AD[21]	AE4	PCI	I/O	Multiplexed Address or Data Bit 21
AD[19]	AE5	PCI	I/O	Multiplexed Address or Data Bit 19
IRDY	AE6	PCI	I/O	Initiator Ready is asserted during writes to indicate valid data on AD[31:0]. Also asserted during reads to indicate the target is prepared to accept data. Wait states are inserted until IRDY and TRDY are both asserted.
STOP	AE7	PCI	I/O	Stop is asserted to indicate a request from the target for the master to stop the current transmission.
C/BE[1]	AE8	PCI	I/O	Multiplexed Command or Byte Enable 1
AD[12]	AE9	PCI	I/O	Multiplexed Address or Data Bit 12
AD[08]	AE10	PCI	I/O	Multiplexed Address or Data Bit 8
AD[05]	AE11	PCI	I/O	Multiplexed Address or Data Bit 5
AD[02]	AE12	PCI	I/O	Multiplexed Address or Data Bit 2
XIO_A25	AE13	MISC	I/O	XIO Address Bit 25
GPIO[7]	AE14	GPIO	I/O	General Purpose Input/Output Bit 7

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
I2S_IO_SCK	AE15	AVIF	I/O	Audio IN/OUT Serial Clock
I2S_IO_SD[1]	AE16	AVIF	I/O	Audio IN/OUT Data Bit 1
DV1_DATA[9]	AE17	DVB	I/O	ITU-656 VIP Data Bit 9 (Most Significant Bit)
DV1_DATA[5]	AE18	DVB	I/O	ITU-656 VIP Data Bit 5
DV1_DATA[2]	AE19	DVB	I/O	ITU-656 VIP Data Bit 2
DV1_CLK	AE20	DVB	I/O	ITU-656 VIP Data Clock
I2S_IN1_SD	AE21	AVIF	I	Audio IN1 Data
I2S_IN2_SD	AE22	AVIF	I	Audio IN2 Data
DV2_DATA[4]	AE23	DVB	I	Digital Video Transport Stream2 Data Bit 4
DV2_DATA[1]	AE24	DVB	I	Digital Video Transport Stream2 Data Bit 1
V _{SS}	AE25	PWR	-	System Ground
V _{SS}	AE26	PWR	-	System Ground
V _{SS}	AF1	PWR	-	System Ground
V _{SS}	AF2	PWR	-	System Ground
IDSEL	AF3	PCI	I/O	Initialization Device Select provides chip select during configuration read and write transactions.
AD[22]	AF4	PCI	I/O	Multiplexed Address or Data Bit 22
C/ $\overline{\text{BE}}$ [2]	AF5	PCI	I/O	Multiplexed Command or Byte Enable 2
FRAME	AF6	PCI	I/O	Frame is asserted to indicate start of bus transaction and remains asserted until final data phase begins.
DEVSEL	AF7	PCI	I/O	Device Select is asserted when a target address is decoded and remains asserted to indicate that a target device is selected.
PAR	AF8	PCI	I/O	Parity supports even parity across the PCI Address/Data Bus AD[31:0]) and Command/ Byte Enable Bus (C/ $\overline{\text{BE}}$ [3:0]). Bus Master drives PAR for address and write data phases. Target drives PAR for the read data phases.
AD[13]	AF9	PCI	I/O	Multiplexed Address or Data Bit 13
AD[09]	AF10	PCI	I/O	Multiplexed Address or Data Bit 9
AD[06]	AF11	PCI	I/O	Multiplexed Address or Data Bit 6
XIO_SEL[2]	AF12	MISC	I/O	External I/O Select2
XIO_ACK	AF13	MISC	I/O	XIO Acknowledge (EEPROM)
GPIO[6]	AF14	GPIO	I/O	General Purpose Input/Output Bit 6
I2S_IO_OSCLK	AF15	AVIF	I/O	Audio IN/OUT OverSample Clock
I2S_IO_SD[2]	AF16	AVIF	I/O	Audio IN/OUT Data Bit 2
SPDIF_IN	AF17	AVIF	I	Multi-ch/SPDIF Input
DV1_DATA[7]	AF18	DVB	I/O	ITU-656 VIP Data Bit 7
DV1_DATA[3]	AF19	DVB	I/O	ITU-656 VIP Data Bit 3
DV1_VALID	AF20	DVB	I/O	ITU-656 VIP Data Valid
I2S_IN1_WS	AF21	AVIF	I/O	Audio IN1 Word Select
I2S_IN2_WS	AF22	AVIF	I/O	Audio IN2 Word Select
DV2_DATA[7]	AF23	DVB	I	Digital Video Transport Stream2 Data Bit 7

Table 16: All pins...continued

Symbol	Pin	Group	Type	Description
DV2_DATA[0]	AF24	DVB	I	Digital Video Transport Stream2 Data Bit 0
V _{SS}	AF25	PWR	-	System Ground
V _{SS}	AF26	PWR	-	System Ground

6.2.1 Multi-function pins

Table 17 identifies and describes alternate signals that are available in the PNX8526. In Section 6.2 alternate signals are also identified by a hash (#) within each functional group of signals.

Remark: The PNX8526 has a number of General Purpose Input Output (GPIO) pins. Some of these are dedicated pins, while others are configured as alternate signals on multi function pins, as described below. The standard function of these pins may not be required in some system configurations.

For more details on GPIO functionality, see *PNX8526 User Manual, Chapter 10*.

Table 17: Multiplexed (MUX) pins

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
AF15	I2S_IO_OSCLK	I/O	Audio IN/OUT Oversample Clock
	GPIO 45	I/O	General Purpose Input/Output 45
AE15	I2S_IO_SCK	I/O	Audio IN/OUT Serial Clock
	GPIO 46	I/O	General Purpose Input/Output 46
AC15	I2S_IO_WS	I/O	Audio IN/OUT Word Select
	GPIO 47	I/O	General Purpose Input/Output 47
AD15	I2S_IO_SD[3]	I/O	Audio IN/OUT Data Bit 3
	GPIO 51	I/O	General Purpose Input/Output 51
AF16	I2S_IO_SD[2]	I/O	Audio IN/OUT Data Bit 2
	GPIO 50	I/O	General Purpose Input/Output 50
AE16	I2S_IO_SD[1]	I/O	Audio IN/OUT Data Bit 1
	GPIO 49	I/O	General Purpose Input/Output 49
AD16	I2S_IO_SD[0]	I/O	Audio IN/OUT Data Bit 0
	GPIO 48	I/O	General Purpose Input/Output 48
R1	DV_CLK2	O	Digital Video Clock2 for secondary display channel from AICP
R2	DV_OUT2[9]	O	Digital Video Output2, Bit 9 for secondary display channel from AICP
	SPY_OUT[9]	O	SPY Micro-Architecture Output signal, Bit 9
R4	DV_OUT2[8]	O	Digital Video Output2, Bit 8 for secondary display channel from AICP
	SPY_OUT[8]	O	SPY Micro-Architecture Output signal, Bit 8
	DSU_TPC1	O	Debug Support Unit1, TPC1
R3	DV_OUT2[7]	O	Digital Video Output2, Bit 7 for secondary display channel from AICP
	SPY_OUT[7]	O	SPY Micro-Architecture Output signal, Bit 7
	DSU_TPC0	O	Debug Support Unit0, TPC0

Table 17: Multiplexed (MUX) pins...continued

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
T1	DV_OUT2[6]	O	Digital Video Output2, Bit 6 for secondary display channel from AICP
	SPY_OUT[6]	O	SPY Micro-Architecture Output signal, Bit 6
	DSU_PCST1[2]	O	Program Counter Status1, Bit 2
T2	DV_OUT2[5]	O	Digital Video Output2, Bit 5 for secondary display channel from AICP
	SPY_OUT[5]	O	SPY Micro-Architecture Output signal, Bit 5
	DSU_PCST1[1]	O	Program Counter Status1, Bit 1
T3	DV_OUT2[4]	O	Digital Video Output2, Bit 4 for secondary display channel from AICP
	SPY_OUT[4]	O	SPY Micro-Architecture Output signal, Bit 4
	DSU_PCST1[0]	O	Program Counter Status1, Bit 0
U1	DV_OUT2[3]	O	Digital Video Output2, Bit 3 for secondary display channel from AICP
	SPY_OUT[3]	O	SPY Micro-Architecture Output signal, Bit 3
	DSU_PCST0[2]	O	Program Counter Status0, Bit 2
T4	DV_OUT2[2]	O	Digital Video Output2, Bit 2 for secondary display channel from AICP
	SPY_OUT[2]	O	SPY Micro-Architecture Output signal, Bit 2
	DSU_PCST0[1]	O	Program Counter Status0, Bit 1
U2	DV_OUT2[1]	O	Digital Video Output2, Bit 1 for secondary display channel from AICP
	SPY_OUT[1]	O	SPY Micro-Architecture Output signal, Bit 1
	DSU_PCST0[0]	O	Program Counter Status0, Bit 0
U3	DV_OUT2[0]	O	Digital Video Output2, Bit 0 for secondary display channel from AICP
	SPY_OUT[0]	O	SPY Micro-Architecture Output signal, Bit 0
	DSU_CLK	O	Debug Support Unit Clock
K2	I2S_OUT2_OSCLK	O	Audio OUT2 Oversample Clock
	DV_OUT[20]	O	AICP RGB Data Bit 20
	SPY_OUT[11]	O	SPY Micro-Architecture Output signal, Bit 11
L3	I2S_OUT2_SCK	I/O	Audio OUT2 Serial Clock
	DV_OUT[21]	O	AICP RGB Data Bit 21
	SPY_OUT[10]	O	SPY Micro-Architecture Output signal, Bit 10
K1	I2S_OUT2_WS	I/O	Audio OUT2 Word Select
	DV_OUT[22]	O	AICP RGB Data Bit 22
	DBG_EXT_STOP	I	External Stop Request signal
L4	I2S_OUT2_SD	O	Audio OUT2 Data
	DV_OUT[23]	O	AICP RGB Data Bit 23 (Most Significant Bit)
	CLK_SPY	O	SPY Micro-Architecture Clock Output signal
AE17	DV1_DATA[9]	I	ITU-656 VIP Data Bit 9 (Most Significant Bit)
	GPIO 42	I/O	General Purpose Input/Output 42
AD17	DV1_DATA[8]	I	ITU-656 VIP Data Bit 8
	GPIO 41	I/O	General Purpose Input/Output 41

Table 17: Multiplexed (MUX) pins...continued

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
AF18	DV1_DATA[7]	I	ITU-656 VIP Data Bit 7
	GPIO 40	I/O	General Purpose Input/Output 40
AC17	DV1_DATA[6]	I	ITU-656 VIP Data Bit 6
	GPIO 39	I/O	General Purpose Input/Output 39
AE18	DV1_DATA[5]	I	ITU-656 VIP Data Bit 5
	GPIO 38	I/O	General Purpose Input/Output 38
AD18	DV1_DATA[4]	I	ITU-656 VIP Data Bit 4
	GPIO 37	I/O	General Purpose Input/Output 37
AF19	DV1_DATA[3]	I	ITU-656 VIP Data Bit 3
	GPIO 36	I/O	General Purpose Input/Output 36
AE19	DV1_DATA[2]	I	ITU-656 VIP Data Bit 2
	GPIO 35	I/O	General Purpose Input/Output 35
AC18	DV1_DATA[1]	I	ITU-656 VIP Data Bit 1
	GPIO 34	I/O	General Purpose Input/Output 34
AD19	DV1_DATA[0]	I	ITU-656 VIP Data Bit 0 (Least Significant Bit)
	GPIO 33	I/O	General Purpose Input/Output 33
AF20	DV1_VALID	I	ITU-656 VIP Data Valid
	GPIO 44	I/O	General Purpose Input/Output 44
AE20	DV1_CLK	I	ITU-656 VIP Data Clock
	GPIO 43	I/O	General Purpose Input/Output 43
AF23	DV2_DATA[7]	I	Digital Video Transport Stream2 Data Bit 7
	VIP[9]	I	ITU-656 VIP Data Bit 9 (Most Significant Bit)
AC21	DV2_DATA[6]	I	Digital Video Transport Stream2 Data Bit 6
	VIP[8]	I	ITU-656 VIP Data Bit 8
	TSS_DATA2	I	Digital Video Transport Stream2 Serial Data2
AD22	DV2_DATA[5]	I	Digital Video Transport Stream2 Data Bit 5
	VIP[7]	I	ITU-656 VIP Data Bit 7
	TSS_SOP2	I	Digital Video Transport Stream2 Serial Start of Packet2
AE23	DV2_DATA[4]	I	Digital Video Transport Stream2 Data Bit 4
	VIP[6]	I	ITU-656 VIP Data Bit 6
	TSS_ERR2	I	Digital Video Transport Stream2 Serial Error2
AC22	DV2_DATA[3]	I	Digital Video Transport Stream2 Data Bit 3
	VIP[5]	I	ITU-656 VIP Data Bit 5
	TSS_VALID2	I	Digital Video Transport Stream2 Serial Valid2
AD23	DV2_DATA[2]	I	Digital Video Transport Stream2 Data Bit 2
	VIP[4]	I	ITU-656 VIP Data Bit 4
	TSS_CLK2	I	Digital Video Transport Stream2 Serial Clock2

Table 17: Multiplexed (MUX) pins...continued

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
AE24	DV2_DATA[1]	I	Digital Video Transport Stream2 Data Bit 1
	VIP[3]	I	ITU-656 VIP Data Bit 3
AF24	DV2_DATA[0]	I	Digital Video Transport Stream2 Data Bit 0
	VIP[2]	I	ITU-656 VIP Data Bit 2
	TSS_DATA1	I	Digital Video Transport Stream2 Serial Data1
AD24	DV2_SOP	I	Digital Video Transport Stream2 Start of Packet
	VIP[1]	I	ITU-656 VIP Data Bit 1
	TSS_SOP1	I	Digital Video Transport Stream2 Serial Start of Packet1
AD26	DV2_ERR	I	Digital Video Transport Stream2 Error
	VIP[0]	I	ITU-656 VIP Data Bit 0 (Least Significant Bit)
	TSS_ERR1	I	Digital Video Transport Stream2 Serial Error1
AD25	DV2_VALID	I	Digital Video Transport Stream2 Data Valid
	VIP_VALID	I	ITU-656 VIP Data Valid
	TSS_VALID1	I	Digital Video Transport Stream2 Serial Valid1
AC24	DV2_CLK	I	Digital Video Transport Stream2 Clock
	VIP_CLK	I	ITU-656 VIP Data Clock
	TSS_CLK1	I	Digital Video Transport Stream2 Serial CLock1
W23	DV3_DATA[7]	I	Digital Video Transport Stream3 Data Bit 7
	VIP[9]	I	ITU-656 VIP Data Bit 9 (Most Significant Bit)
Y24	DV3_DATA[6]	I	Digital Video Transport Stream3 Data Bit 6
	VIP[8]	I	ITU-656 VIP Data Bit 8
	TSS_DATA2	I	Digital Video Transport Stream3 Serial Data2
Y25	DV3_DATA[5]	I	Digital Video Transport Stream3 Data Bit 5
	VIP[7]	I	ITU-656 VIP Data Bit 7
	TSS_SOP2	I	Digital Video Transport Stream3 Serial Start of Packet2
Y26	DV3_DATA[4]	I	Digital Video Transport Stream3 Data Bit 4
	VIP[6]	I	ITU-656 VIP Data Bit 6
	TSS_ERR2	I	Digital Video Transport Stream3 Serial Error2
W24	DV3_DATA[3]	I	Digital Video Transport Stream3 Data Bit 3
	VIP[5]	I	ITU-656 VIP Data Bit 5
	TSS_VALID2	I	Digital Video Transport Stream3 Serial Valid2
V23	DV3_DATA[2]	I	Digital Video Transport Stream3 Data Bit 2
	VIP[4]	I	ITU-656 VIP Data Bit 4
	TSS_CLK2	I	Digital Video Transport Stream3 Serial Clock2
W25	DV3_DATA[1]	I	Digital Video Transport Stream3 Data Bit 1
	VIP[3]	I	ITU-656 VIP Data Bit 3

Table 17: Multiplexed (MUX) pins...continued

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
W26	DV3_DATA[0]	I	Digital Video Transport Stream3 Data Bit 0
	VIP[2]	I	ITU-656 VIP Data Bit 2
	TSS_DATA1	I	Digital Video Transport Stream3 Serial Data1
V24	DV3_SOP	I	Digital Video Transport Stream3 Start of Packet
	VIP[1]	I	ITU-656 VIP Data Bit 1
	TSS_SOP1	I	Digital Video Transport Stream3 Serial Start of Packet1
U23	DV3_ERR	I	Digital Video Transport Stream3 Error
	VIP[0]	I	ITU-656 VIP Data Bit 0 (Least Significant Bit)
	TSS_ERR1	I	Digital Video Transport Stream3 Serial Error1
V25	DV3_VALID	I	Digital Video Transport Stream3 Data Valid
	VIP_VALID	I	ITU-656 VIP Data Valid
	TSS_VALID1	I	Digital Video Transport Stream3 Serial Valid1
V26	DV3_CLK	I	Digital Video Transport Stream3 Clock
	VIP_CLK	I	ITU-656 VIP Data Clock
	TSS_CLK1	I	Digital Video Transport Stream3 Serial Clock1
AB23	TS_DATA[7]	O	Transport Stream Data Bit 7
	GPIO 29	I/O	General Purpose Input/Output 29
AC25	TS_DATA[6]	O	Transport Stream Data Bit 6
	GPIO 28	I/O	General Purpose Input/Output 28
AB24	TS_DATA[5]	O	Transport Stream Data Bit 5
	GPIO 27	I/O	General Purpose Input/Output 27
AA23	TS_DATA[4]	O	Transport Stream Data Bit 4
	GPIO 26	I/O	General Purpose Input/Output 26
AC26	TS_DATA[3]	O	Transport Stream Data Bit 3
	GPIO 25	I/O	General Purpose Input/Output 25
AB25	TS_DATA[2]	O	Transport Stream Data Bit 2
	GPIO 24	I/O	General Purpose Input/Output 24
AB26	TS_DATA[1]	O	Transport Stream Data Bit 1
	GPIO 23	I/O	General Purpose Input/Output 23
Y23	TS_DATA[0]	O	Transport Stream Data Bit 0
	GPIO 22	I/O	General Purpose Input/Output 22
	TS_SD	O	Transport Stream Serial Data Out
AA24	TS_SOP	O	Transport Stream Start of Packet (Parallel/Serial)
	GPIO 31	I/O	General Purpose Input/Output 31
AA25	TS_VALID	O	Transport Stream Data Valid (Parallel/Serial)
	GPIO 32	I/O	General Purpose Input/Output 32
AA26	TS_CLK	O	Transport Stream Clock (Parallel/Serial)
	GPIO 30	I/O	General Purpose Input/Output 30

Table 17: Multiplexed (MUX) pins...continued

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
AA2	PCI_REQ_A*[1]	I/O	Auxiliary Arbitration REQ_A on PCI Bus. Used in modes where internal arbiter is configured.
	GPIO 57	I/O	General Purpose Input/Output 57
AA3	PCI_REQ_B*	I/O	Auxiliary Arbitration REQ_B on PCI Bus. Used in modes where internal arbiter is configured.
	GPIO 58	I/O	General Purpose Input/Output 58
Y4	PCI_GNT_A*	I/O	Auxiliary Arbitration Grant_A is asserted to indicate bus access has been granted to an external PCI master. Used where internal arbiter is configured.
	GPIO 59	I/O	General Purpose Input/Output 59
AA4	PCI_GNT_B*	I/O	Auxiliary Arbitration Grant_B is asserted to indicate bus access has been granted to an external PCI master. Used where internal arbiter is configured.
	GPIO 60	I/O	General Purpose Input/Output 60
AF12	XIO_SEL[2]*	O	External MMIO Select 2
	GPIO 54	I/O	General Purpose Input/Output 54
AC13	XIO_SEL[1]*	O	External MMIO Select 1
	GPIO 53	I/O	General Purpose Input/Output 53
AD13	XIO_SEL[0]*	O	External MMIO Select 0
	GPIO 52	I/O	General Purpose Input/Output 52
AF13	XIO_ACK*	I	XIO Acknowledge (EEPROM)
	GPIO 55	I/O	General Purpose Input/Output 55
AE13	XIO_A25*	O	XIO Address bit 25
	GPIO 56	I/O	General Purpose Input/Output 56
U24	UA1_TX	O	UART1 Transmit
	GPIO 12	I/O	General Purpose Input/Output 12
U25	UA1_RX	I	UART1 Receive
	GPIO 13	I/O	General Purpose Input/Output 13
T23	UA2_TX	O	UART2 Transmit
	GPIO 14	I/O	General Purpose Input/Output 14
U26	UA2_RX	I	UART2 Receive
	ICAM1_SETVPP	O	ICAM1 VPP**[2]
	GPIO 15	I/O	General Purpose Input/Output 15
T24	UA2_RTSN	O	UART2 Request To Send
	ICAM1_C8	I	ICAM1 C8**
	GPIO 16	I/O	General Purpose Input/Output 16
T25	UA2_CTSN	I	UART2 Clear To Send
	ICAM1_C4	I/O	ICAM1 C4
	GPIO 17	I/O	General Purpose Input/Output 17

Table 17: Multiplexed (MUX) pins...continued

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
V1	SSI_SCLK_CTSN	I	Synchronous Serial Interface CLock Input
	UART CTS	I	UART2 Clear To Send
	GPIO 21	I/O	General Purpose Input/Output 21
V2	SSI_FS_RTSN	I	Synchronous Serial Interface Frame Sync
	UART RTS	O	UART2 Request To Send
	GPIO 20	I/O	General Purpose Input/Output 20
U4	SSI_RXD	I	Synchronous Serial Interface Receive
	GPIO 19	I/O	General Purpose Input/Output 19
V3	SSI_TXD	O	Synchronous Serial Interface Transmit
	GPIO 18	I/O	General Purpose Input/Output 18
N26	ICAM2_C4	I/O	ICAM2 C4
	GPIO 11	I/O	General Purpose Input/Output 11
N24	ICAM2_C8	I/O	ICAM2 C8
	GPIO 10	I/O	General Purpose Input/Output 10
N23	ICAM2_SETVPP	O	ICAM2 VPP
	GPIO 9	I/O	General Purpose Input/Output 9
M26	GPIO 8	I/O	General Purpose Input/Output 8
AE14	GPIO 7	I/O	General Purpose Input/Output 7
AF14	GPIO 6	I/O	General Purpose Input/Output 6
AD14	GPIO 5	I/O	General Purpose Input/Output 5
AC14	GPIO 4	I/O	General Purpose Input/Output 4
C5	GPIO 3	I/O	General Purpose Input/Output 3
B4	Boot Mode [2]	I	Select Configuration Bit 2 during System Reset
	GPIO 2	I/O	General Purpose Input/Output 2
D5	Boot Mode [1]	I	Select Configuration Bit 1 during System Reset
	GPIO 1	I/O	General Purpose Input/Output 1
C4	Boot Mode [0]	I	Select Configuration Bit 0 during System Reset
	GPIO 0	I/O	General Purpose Input/Output 0
P25	SC2_OFFN	I	Smartcard Off
	ICAM2_DETECT	I	ICAM2 Detect
P24	SC2_CMD	O	Smartcard Command
	ICAM2_SETVCC	O	ICAM2 VCC
P26	SC2_RST	O	Smartcard Reset
	ICAM2_RESET	O	ICAM2 Reset
N25	SC2_SCCK	O	Smartcard Clock
	ICAM2_CLK	O	ICAM2 Clock
P23	SC2_DA	I/O	SmartCard2 Data
	ICAM2_C7	I/O	ICAM2 C7

Table 17: Multiplexed (MUX) pins...continued

In this table, "Type" reflects mux pin function only. A pin may have other "Type" capabilities as noted in its functional group. See Section 6.2 for more details.

Pin	MUX contacts Primary signal and Alternate Function	Type	Description
R25	SC1_OFFN	I	Smartcard Off
	ICAM1_DETECT	I	ICAM1 Detect
R23	SC1_CMD	O	Smartcard Command
	ICAM1_SETVCC	O	ICAM1 VCC
R24	SC1_RST	O	Smartcard Reset
	ICAM1_RESET	O	ICAM1 Reset
R26	SC1_SCCK	O	Smartcard Clock
	ICAM1_CLK	O	ICAM1 Clock
T26	SC1_DA	I/O	Smartcard1 Data
	ICAM1_C7	I/O	ICAM1 C7

[1] *These pins are included in the XIO set. Refer to *PNX8526 User Manual, Chapter 8* for additional functions.

[2] **The ICAM1_SETVPP and ICAM1_C8 signals are automatically selected when the ICAM function is selected. Refer to [Table 18](#) (Offset 0x04 D600 IO_MUX_CTR). Selecting GPIO mode will disable this ICAM functionality.

7. Functional description

[Figure 3](#) shows a block diagram of a typical PNX8526-based system. The system shown is a "standalone system" which uses the internal MIPS host.

The PNX8526 runs on a single 27 MHz xtal from which all internal and external clocks are derived by on-chip synthesizers. The PNX8526 boots directly from attached Flash memory or ROM. If desired, custom boot methods can be programmed using the optional I²C boot EEPROM.

The PNX8526 has three Digital Video inputs that accept digitized analog video (ITU-656), although only two ITU-656 streams can be processed simultaneously. Two of these inputs, DV2 and DV3, can also accept scrambled transport streams.

The DV inputs support parallel transport stream formats. In addition, a single incoming 1394 transport stream is supported. Two selected transport streams can undergo internal de-scrambling and decoding.

Based on the system implementation, one or both transport streams may pass through Point of Deployment (POD) or Common Interface (CI) conditional access modules before transfer into the PNX8526. Either a single companion IC, such as the SCM Microsystems CIMaX™, or two CIMaX™ chips can be used. In the latter case, it is possible to handle dual decoding no matter which conditional access system is used.

The PNX8526 contains on-chip DVB, MULTI2 and DES hardware de-scramblers, as well as an ICAM verifier. The entitlement system for these de-scramblers is provided via two Smartcard interfaces.

The TM32 CPU does further processing on the result of the transport stream de-mux.

For MPEG2 video, a slice level HL MPEG2 video decoder performs the majority of the MPEG2 algorithm. This MPEG decoder is capable of full-resolution decoding. The TM32 CPU does all MPEG2 processing above the slice level. Two simultaneous SD streams or one HD stream may be processed.

All audio processing is done by the TM32 CPU. Compressed audio will be present in memory from either the transport stream de-multiplex or from the SPDIF input port. The SPDIF input port is intended primarily for DTV applications where a SPDIF source is available from an external source device, such as a DVD player. PCM (stereo sample) audio is present in memory from the I²S input ports or SPDIF input. Two AC-3 (or equivalent) compressed audio streams may be decoded simultaneously. The TM32 CPU may also process effects, enhancements and mix the audio data. Multi-channel compressed audio or down-mixed stereo PCM audio is transmitted over the SPDIF output interface. Multi-channel audio samples are Dolby Pro Logic™ down-mixed into the two stereo I²S interfaces to the PNX8510 companion IC. In addition to the two I²S inputs and two I²S outputs, a bi-directional I²S interface is provided. This allows connection of other audio inputs or outputs— headphones, for example. Note that there is not enough compute power to support encoding of multi-channel compressed audio simultaneous with video processing. So the multi-channel compressed audio transmitted over SPDIF must be from one of the original compressed sources.

Graphics rendering may be accomplished with the MIPS or the TM32 CPU by utilizing the 2D Drawing and DMA engine. This engine can perform fast area fills, 3-operand bitblt, monochrome data expansion, and lines. It can also be used as a generic DMA engine to transfer data between memory locations on a byte-aligned basis. An alpha bitblt capability is also provided to allow for anti-aliased text and lines as well as source/destination blending operations.

Once all video and graphics data for specific fields or frames has been generated in memory, the video display pipeline starts processing those images for display. The video processing functions include 6-tap horizontal/vertical scaling, anti-flicker filtering, and de-interlacing (when progressive output is required). The processed images are then combined for each output. Up to four surfaces of any supported format may be combined to produce the primary display output. Up to two surfaces are combined to produce the secondary output. Compositing of more surfaces for future video algorithms is possible by using the TM32 CPU and/or the memory based scaler prior to invoking the compositing/display engine. This is subject to CPU and memory bandwidth availability.

The PNX8526 contains a 1394 interface with 5C copy protection. The PNX8526 1394 can simultaneously transmit two transport streams while receiving one transport stream. The transmitted streams can be partial transport streams (created by PID filtering of an input) or one of the two streams can be software generated. In the case of receiving a scrambled 1394 transport stream input, the stream can either use the on-chip de-scramblers, or may be routed to the external companion CA IC for de-scrambling by the POD/CI CA module(s).

The PNX8526 contains a variety of peripheral interfaces to support both ASTB and DTV requirements. There are two Smartcard interfaces, two USB ports, two I²C ports, one IrDA Data UART and two general purpose UARTs, one of which (UART3) is multiplexed with an SSI interface for soft modem support. The PNX8526 also contains an integrated IDE controller, which only requires an external isolation buffer

to implement a full disk interface with sustained speeds up to 10 MB/s. A third-party PCI Super I/O chip may be utilized to provide peripheral functionality not contained on the PNX8526. Functions such as IEEE-1284, 10/100 Ethernet, floppy drive support, UDMA66 IDE controllers and others are currently available in low-cost, commercially available parts.

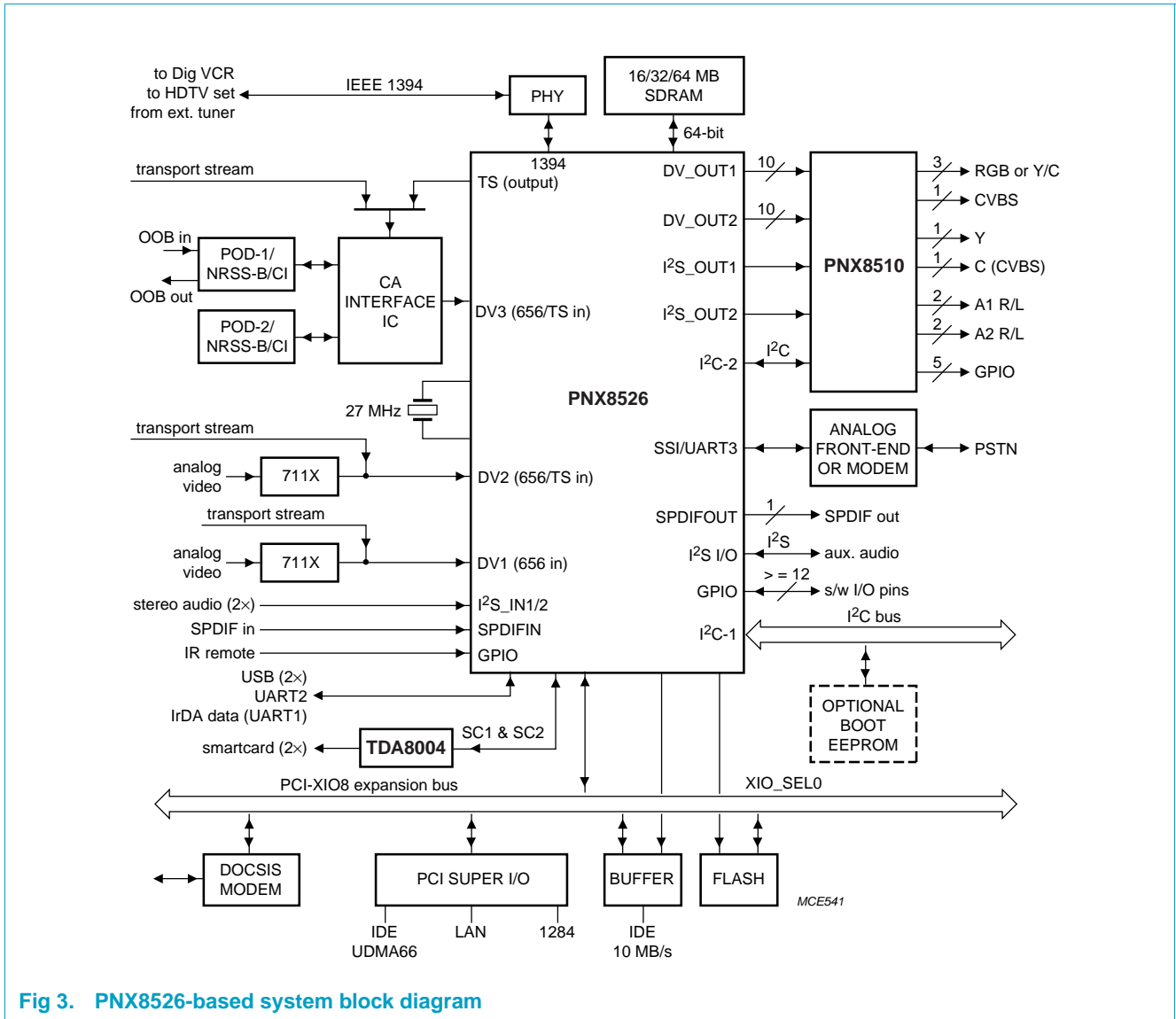


Fig 3. PNX8526-based system block diagram

8. I/O multiplexer control register

The I/O Multiplexer Control register is used to configure the multi function pins to alternate functions as described in Table 17. Control is achieved via the Global 2 register IO_MUX_CTRL Table 18.

Table 18: Global 2 registers

Bit	Symbol	Access	Value	Description
0x04 D600 IO_MUX_CTRL				
31:15	Not used			Ignore during writes and read as zeroes.
14	AIO_MUX_SEL	R/W	0x0	I2S_IO Audio mode: 0 = Select I2S_IO as Audio Out. 1 = Select I2S_IO as Audio In.
13	SSI_SEL	R/W	0x0	SSI or UART3 mode: 0 = Select UART3. 1 = Select SSI.
12	RGB24_SEL	R/W	0x0	Audio Out2 or RGB mode: 0 = Select Audio Out2. 1 = Select RGB (DV_OUT [23:20]).
11:10	SMCRD2_MUX_CTRL	R/W	0x0	ICAM or SmartCard2 mode: 00 = SmartCard1 module ports go to SmartCard2 pins. 01 = SmartCard2 module ports go to SmartCard2 pins. 10 = ICAM1 module ports go to SmartCard2 pins. 11 = ICAM2 module ports go to SmartCard2 pins.
9:8	SMCRD1_MUX_CTRL	R/W	0x0	ICAM or SmartCard2 mode: 00 = SmartCard1 module ports go to SmartCard1 pins. 01 = SmartCard2 module ports go to SmartCard1 pins. 10 = ICAM1 module ports go to SmartCard1 pins. 11 = ICAM2 module ports go to SmartCard1 pins.
7	Not used		-	Ignore during writes and read as zeroes.
6:4	VIP2_MUX_CTRL[2:0]	R/W	0x0	VIP2 module selection: 000 = VIP data from DV1 port 001 = VIP data from DV2 port 010 = VIP data from DV3 port 011 = VIP data from DV_OUT1(AICP1) port 100 = 1394 data from link core
3	Not used		-	Ignore during writes and read as zeroes.
2:0	VIP1_MUX_CTRL[2:0]	R/W	0x0	VIP1 module selection: 000 = VIP data from DV1 port 001 = VIP data from DV2 port 010 = VIP data from DV3 port 011 = VIP data from DV_OUT2 (AICP2) port 100 = 1394 data from link core

9. Power supply sequencing

Power application and power removal should obey the following rules:

9.1 Power on sequence

- Apply power to V_{DD} 1.26 V
- Allow V_{DD} 1.26 V to stabilize (approx. 100 ms recommended)
- Apply power to V_{DD} 3.3 V

9.2 Power off sequence

- Power may be removed from V_{DD} 3.3 V and V_{DD} 1.26 V at the same time
- Otherwise remove V_{DD} 3.3 V followed by 1.26 V

10. Limiting values

Table 19: Maximum ratings

Symbol	Parameter	Min	Max	Typical	Unit
T_{amb}	Ambient temperature	0	70	-	°C
T_{stg}	Storage temperature	-40	+125	-	°C
T_j	Junction temperature	-	100	-	°C
	3-volt I/O pin voltage with respect to V_{SS}	-0.5	$V_{DD}+0.5$	-	V
	5-volt tolerant I/O pin voltage with respect to V_{SS}	-0.5	5.5	-	V
	I/O with Non-Schmitt trigger input voltage threshold	1.46	1.76	-	V
	I/O with Schmitt trigger input threshold VILT	0.93	1.06	-	V
	I/O with Schmitt trigger input threshold VIHT	1.66	1.79	-	V
	I/O transient pin voltage	-	10	-	V
	DC supply voltage (V_{DD} I/O pad)	3.0	3.6	-	V
	DC supply voltage (V_{DDC} core logic)	1.20	1.32	-	V
	Dynamic Power Dissipation	-	2	-	W
	Static Power Dissipation (AICP off)	-	1	-	W
	Electrostatic Discharge (Human Body Model)	-	± 1.5	-	kV

11. Thermal characteristics

PNX8526 can be used in different environments creating different junction temperatures.

The thermal resistance from junction to ambient (i.e. θ_{ja}) of the PNX8526 in its HBGA456 package is around 11.7 C/W. This value is achieved using natural convection, no external heatsink and using a JEDEC defined high-conductive board (see JEDEC standards 51-2 and 51-7 for details).

Given the power dissipation of the PNX8526 and the ambient temperature inside the enclosure, the expected junction temperature can be calculated using the following equation:

$$T_j = T_{amb} + P \times R_{th(j-a)}$$

In some applications the junction temperature may be judged too high, reducing the acceptable lifetime (see [Section 15](#)). However cooling can be improved by fitting an additional external heatsink, or increasing the airflow around the device. [Table 20](#) shows the improvements that can be expected if these measures are taken.

Table 20: PNX8526 thermal data

Heatsink size = 37 x 37 x 10 mm

PNX8526	Thermal resistance $R_{th(j-a)}$ (C/W)		
	Airflow		
	0 m/s	1 m/s	2 m/s
Standard	11.7	10.0	8.5
With external h'sink	9.5	7.6	6.3

12. Static characteristics

The characteristics listed in the following tables apply to standard operating conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin. The standard operating voltage range is $V_{DD} = 3.3 \pm 0.3 V_{DC}$ and $V_{DDC} = 1.26 \pm 0.06 V_{DC}$. All digital I/O pins are 3.3 V tolerant.

In all cases described below, digital $V_{DD} = 3.3 V + 5\%$ and operating temperature is 0° to $70^\circ C$.

All AC timings are based on a 30 pF test load and are measured at a 1.6 V threshold (see [Figure 4](#)) Actual I/O voltage threshold is dependant on pad type e.g., Schmitt trigger input (see [Section 6.1](#)).

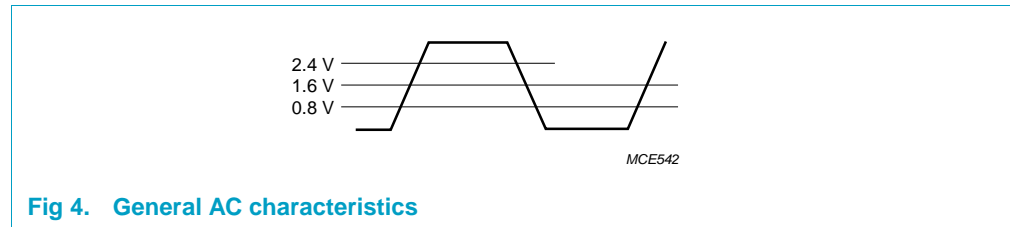


Fig 4. General AC characteristics

The AC voltage characteristics for active signal pins of the controller are listed in [Table 21](#). Signal names for the PCI bus configuration are listed, as well as the minimum and maximum voltage, current, and capacitance for each pin.

Table 21: Digital AC/DC characteristics

Symbol	Parameter	Min	Max	Typical	Unit
V_{IL}	Input Low Voltage	-0.5	+0.8	-	V
V_{IH}	Input High Voltage	2.4	$V_{dd} + 0.5$	-	V
V_{OL}	Output Low Voltage	V_{ss}	$V_{ss} + 0.4$	-	V
V_{OH}	Output High Voltage	2.4	-	-	V
$I_{OL1}^{[1]}$	Output Low Current	-	5	-	mA
I_{OH1}	Output High Current	-	-5	-	mA
$I_{OL2}^{[2]}$	Output Low Current	-	8	-	mA
I_{OH2}	Output High Current	-	-8	-	mA
$I_{OL3}^{[3]}$	Output Low Current	-	12	-	mA
I_{OH3}	Output High Current	-	-12	-	mA
$I_{OL4}^{[4]}$	Output Low Current	-	14	-	mA
I_{OH4}	Output High Current	-	-14	-	mA

Table 21: Digital AC/DC characteristics...continued

Symbol	Parameter	Min	Max	Typical	Unit
I _{OZ}	Output Tri-state Current	-	0.041	-	mA
C _{IN} , C _{OUT} , C _{I/O}	Input Capacitance	-	3.5	-	pF
I _{CC}	Power Supply Current	-	1.5	0.9	A
I _{CP}	Power Supply Current	-	0.2	0.13	A

- [1] I_{OL1} (4mA):
I2S_IN1_SCK, I2S_IN1_WS, I2S_IN2_SCK, I2S_IN2_WS, I2S_OUT1_SCK, I2S_OUT1_WS, I2S_OUT1_SD, I2S_OUT2_SD, DV1_DATA[9:0], DV1_VALID, DV1_CLK, DBG_TDO, JTAG_TDO, XTAL_OUT, UA1_TX, UA1_RX, UA2_TX, UA2_RX, UA2_RTS, UA2_CTS, SC1_DA, SC1_CMD, SC1_RST, SC1_SCCK, SC2_DA, SC2_CMD, SC2_RST, SC2_SCCK, SSI_SCLK_CTSN, SSI_FS_RTSN, SSI_RX, SSI_TX, USB_DM[1:0], USB_DP[1:0], USB_BUS_PWR
- [2] I_{OL2} (8mA):
DV_OUT1[9:0], DV_OUT2[9:0], DV_CLK1, DV_CLK2, HSYNC, VSYNC, BLANK, I2S_IN1_OSCLK, I2S_IN2_OSCLK, I2S_IO_OSCLK, I2S_IO_SCK, I2S_IO_WS, I2S_IO_SD[3:0], I2S_OUT1_OSCLK, I2S_OUT2_OSCLK, I2S_OUT2_SCK, I2S_OUT2_WS, TS_DATA[7:0], TS_SOP, TS_VALID, TS_CLK, PHY_DATA[7:0], PHY_CTL[1:0], PHY_LREQ, MM_DATA[63:0], MM_DQMM_[7:0], MM_CKE, I2C1_SCL, I2C1_SDA, I2C2_SCL, I2C2_SDA, GPIO[11:0], SYS_RSTN_OUT, XIO_SEL[2:0], XIO_ACK, XIO_AD25
- [3] I_{OL3} (12mA):
PCI_AD[31:0], PCI_CBE[3:0], PCI_DEVSEL, PCI_FRAME, PCI_IRDY, PCI_TRDY, PCI_STOP, PCI_PERR, PCI_PAR, PCI_INTA, PCI_REQ, PCI_GNT, PCI_REQ_A, PCI_REQ_B, PCI_GNT_A, PCI_GNT_B, PCI_SERR, MM_WE, PLL_OUT,
- [4] I_{OL4} (14mA):
SPDIF_OUT, MM_CLK[1:0], MM_ADDR[11:0], MM_BA[1:0], MM_CS, MM_RAS, MM_CAS

The pin names used in the above notes are the primary names for PCI configurations. Output signals multiplexed on some pins have the same drive level. V_{DD} = 3.3 V +5%, Operating Temperature 0 °C to 70 °C

13. Dynamic characteristics

13.1 Reset timing

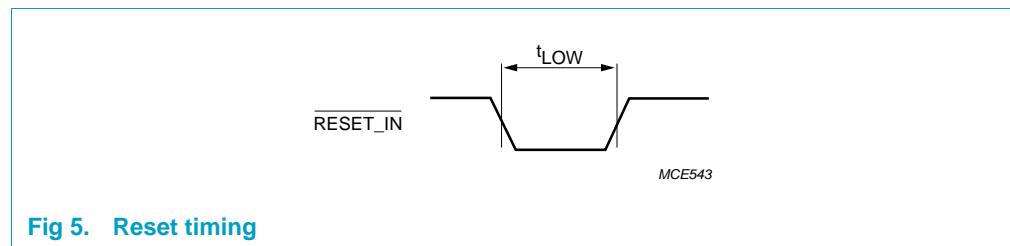


Fig 5. Reset timing

Table 22: Reset timing

Symbol	Parameter	Min	Units
t _{LOW}	RESET_IN active pulse width (after stable power)	400	µs

13.2 Peripheral Controller Interface (PCI) timing

For additional timing diagram information on XIO and IDE interfaces, see PNX8526 User Manual, Chapter 8.

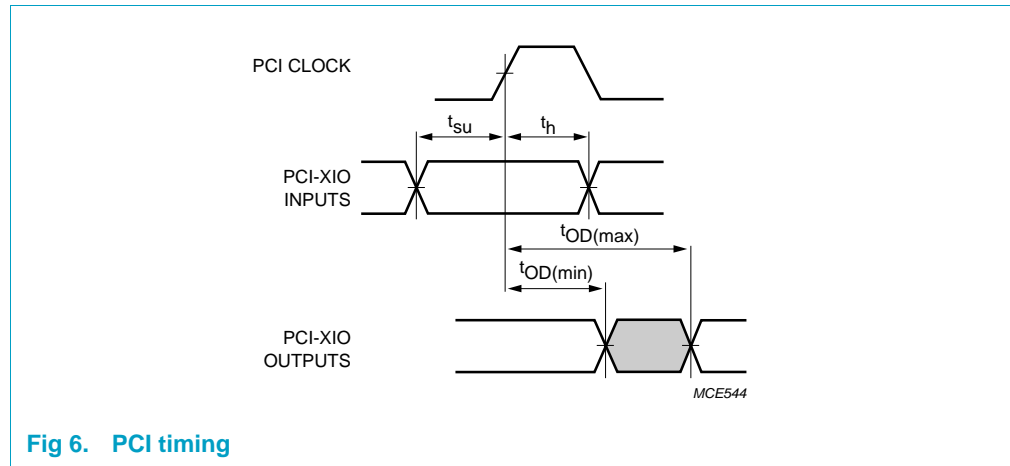


Fig 6. PCI timing

Table 23: PCI CLK-referenced input timing

Symbol	Parameter	Min	Unit
t_{su}	PCI_AD[31:0], CBE[3:0], PCI_FRAME, PCI_IRDY	7	ns
t_h	PCI_AD[31:0] hold	0	ns
t_h	PCI_C/BE[3:0], PCI_FRAME, PCI_IRDY, PCI_IDSEL hold	0	ns
t_{su}	PCI_GNT setup	10	ns
t_h	PCI_GNT hold	0	ns

Table 24: PCI CLK-referenced output valid timing

Symbol	Parameter	Min	Max	Unit
t_{OD}	PCI_AD[31:0], PCI_CBE[3:0]	2	11	ns
t_{OD}	PCI_DEVSEL, PCI_PAR	2	11	ns
t_{OD}	PCI_STOP	2	11	ns
t_{OD}	PCI_TRDY	2	11	ns
t_{OD}	PCI_REQ	2	12	ns

[1] Minimum delay is the minimum time after the clock edge that a valid signal state from the previous cycle will begin transition to the next state (become invalid). Maximum delay is the maximum time after the clock edge that a signal state is valid for the next cycle.

13.3 Main Memory Interface (MMI) timing

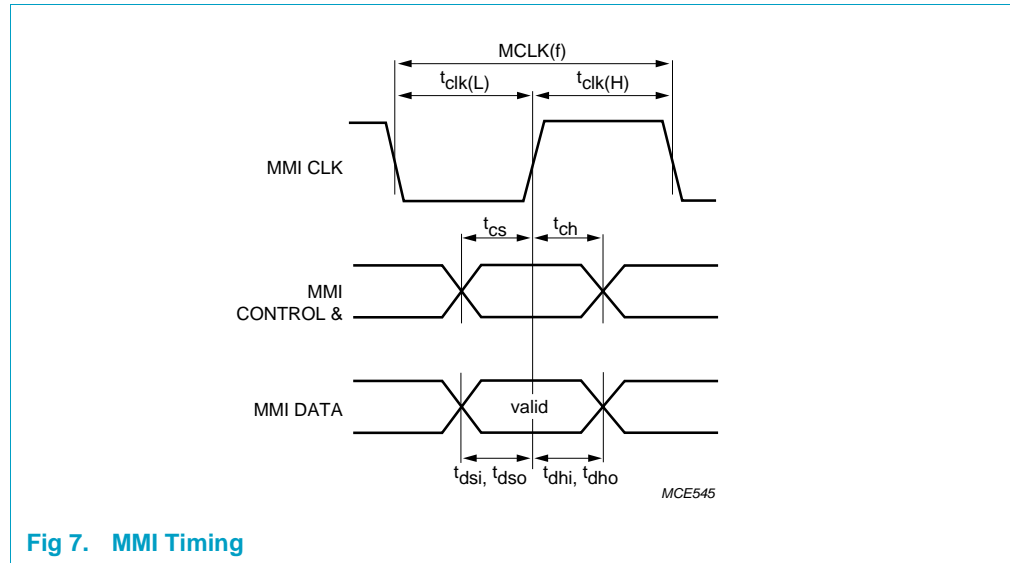


Fig 7. MMI Timing

Table 25: MMI timing (MCLK-referenced)

Symbol	Parameter	Min	Max	Unit
t _{cs}	Setup time with reference to clock	1.5	-	ns
t _{ch}	Hold time with reference to clock	0.8	-	ns
t _{dso}	MMI data output setup time with reference to clock (write cycle)	1.5	-	ns
t _{dho}	MMI data output hold time with reference to clock (write cycle)	0.8	-	ns
t _{dsi}	MMI data input setup with reference to clock (read cycle)	0	-	ns
t _{dhi}	MMI data input hold with reference to clock (read cycle)	2.0	-	ns
t _{clk(L)}	Clock low time	2.9	-	ns
t _{clk(H)}	Clock high time	2.9	-	ns
MCLK(f)	MMI_CLK[1:0]	-	166	MHz

13.4 General Purpose Input/Output (GPIO) timing

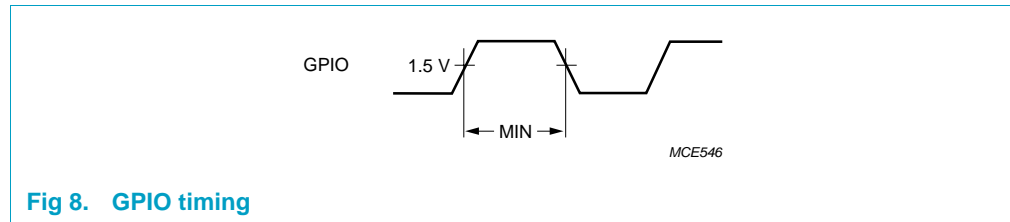


Fig 8. GPIO timing

Table 26: GPIO timing

Parameter	Min	Max	Unit
GPIO as input	10	-	ns ^[1]
GPIO as output	75	-	ns

[1] If GPIO is intended to be timestamped, the minimum pulse width is 75 ns

13.5 Universal Asynchronous Receiver/Transmitter (UART) timing

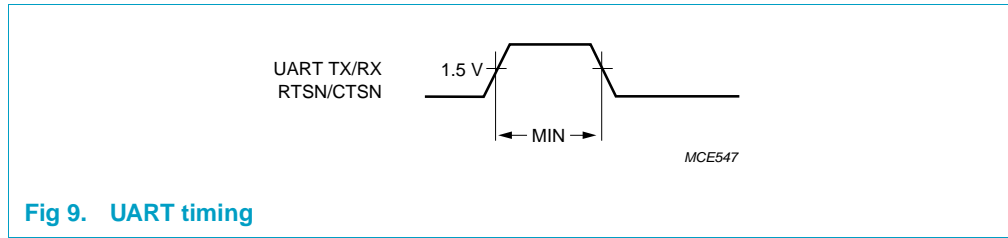


Fig 9. UART timing

Table 27: UART CLK-referenced output timing

Parameter	Min	Max	Unit
UART TX	4.3	-	μs ^[1]
UART RX	4.3	-	μs
UART RTSN	4.3	-	μs
UART CTSN	4.3	-	μs

[1] Max baud rate: 230 kBs

13.6 Synchronous Serial Interface (SSI) timing

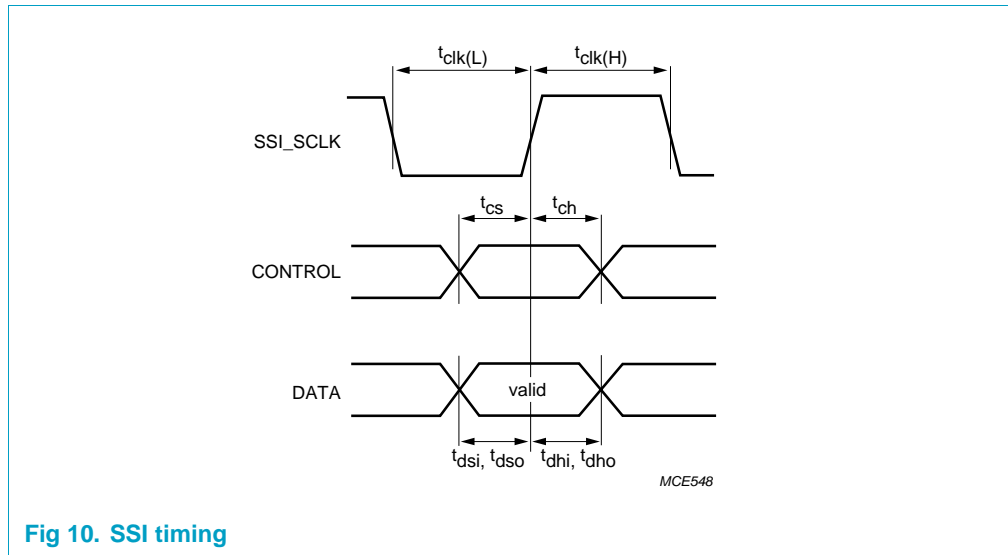


Fig 10. SSI timing

Table 28: SSI interface timing (MCLK-referenced)

Symbol	Parameter	Min	Max	Unit
t_{cs}	Setup time with reference to clock	3	-	ns
t_{ch}	Hold time with reference to clock	2	-	ns
t_{ds0}	Data output setup time with reference to clock	3	-	ns
t_{dho}	Data output hold time with reference to clock	2	-	ns
t_{dsi}	Data input setup with reference to clock	1.0	-	ns
t_{dhi}	Data input hold with reference to clock	1.0	-	ns
$t_{clk(L)}$	Clock low time	25	-	ns
$t_{clk(H)}$	Clock high time	25	-	ns

13.7 I²C-bus timing

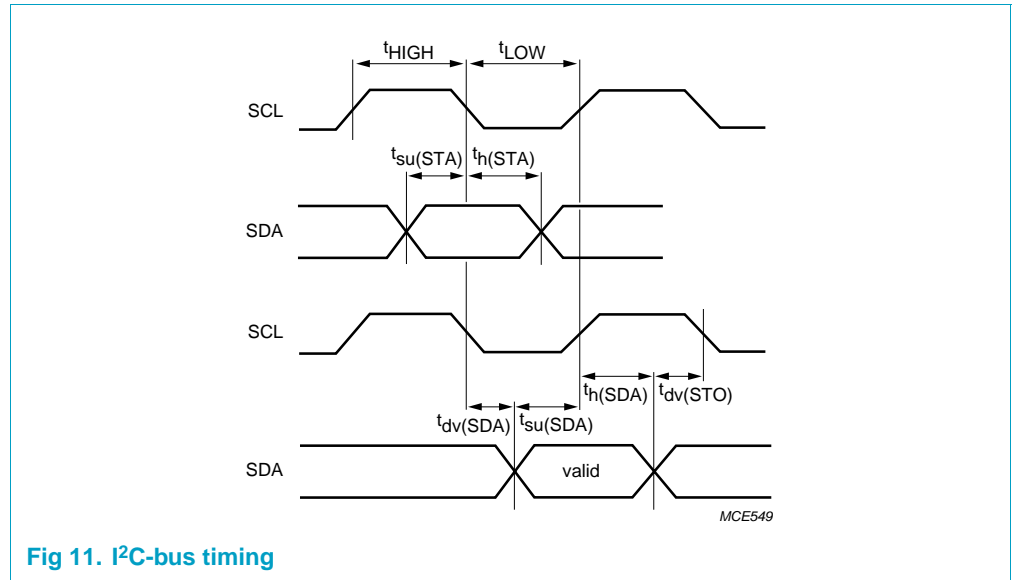


Fig 11. I²C-bus timing

Table 29: I²C-bus timing

Symbol	Parameter	Min	Max	Unit
SCL	SCL clock frequency	-	400	kHz
$t_{su}(STA)$	Start condition setup time	1	-	μ s
$t_h(STA)$	Start condition hold time	1	-	μ s
t_{LOW}	SCL LOW time	1	-	μ s
t_{HIGH}	SCL HIGH time	1	-	μ s
$t_{su}(SDA)$	Data setup time	100	-	ns
$t_h(SDA)$	Data hold time	0	-	ns
$t_{dv}(SDA)$	SCL LOW to data out valid	-	0.5	μ s
$t_{dv}(SDO)$	SCL HIGH to data out	1	-	μ s

13.8 IEEE 1394 Phy-Link interface

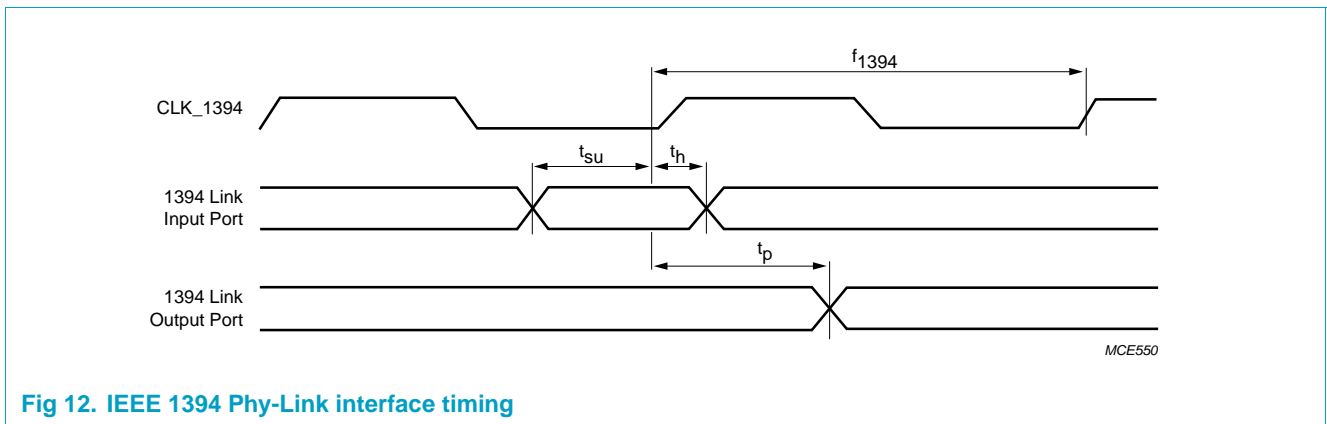


Fig 12. IEEE 1394 Phy-Link interface timing

Table 30: IEEE 1394 Phy-Link interface signals

Symbol	Parameter	Min	Max	Unit
f_{1394}	CLK_1394 frequency	49.147	49.157	MHz
t_{su}	Input setup time for PHY_DATA[7:0], PHY_CTL[1:0]	6	-	ns
t_h	Input hold time	0	-	ns
t_p	Output propagation delay for PHY_DATA[9:0], PHY_LREQ, PHY_CTL[1:0]	-	9	ns

13.9 I2S audio input & output timing

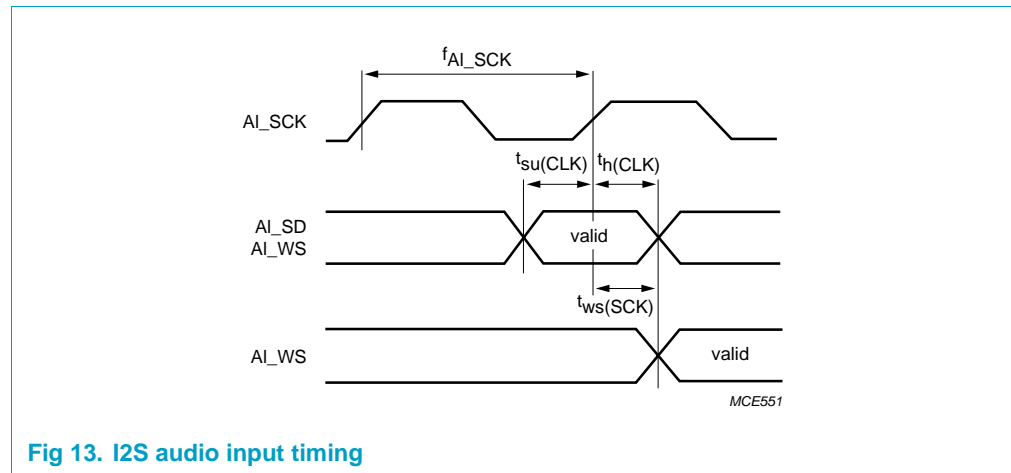


Fig 13. I2S audio input timing

Table 31: I2S audio input

Symbol	Parameter	Min	Max	Unit
f_{AI_SCK}	Audio In AI_SCK clock frequency	-	20	MHz
$t_{su}(CLK)$	Input Setup Time to AI_SCK (Audio interface as slave)	3	-	ns
$t_h(CLK)$	Input Hold Time from AI_SCK (Audio interface as slave)	2	-	ns
$t_{ws}(SCK)$	AI_SCK to AI_WS	2	10	ns

[1] Timing measurements are done with respect to the SCK clock edge. The PNX8526 is the source of AI_WS.

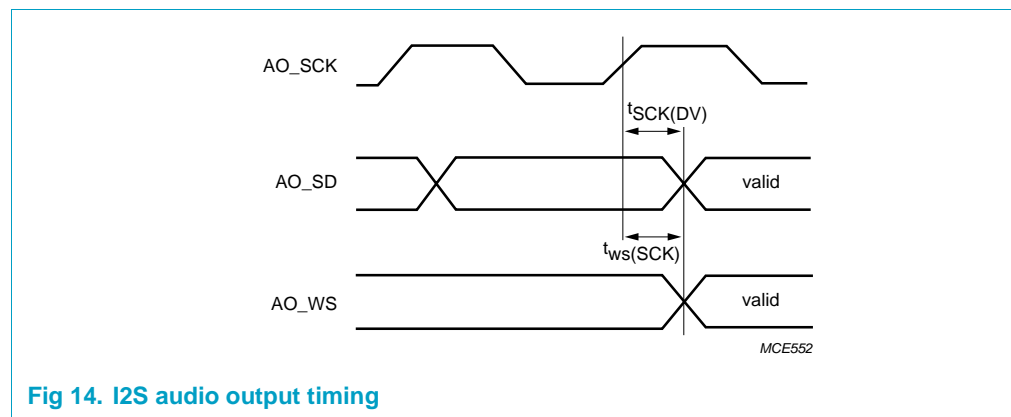


Fig 14. I2S audio output timing

Table 32: I2S audio output

Symbol	Parameter	Min	Max	Unit
AO_SCK	Audio Out to AO_SCK clock frequency	-	20	MHz
$t_{SCK(DV)}$	AO_SCK to AO_SC valid	2	-	ns
$t_{su(SCK)}$	Input Setup Time to AO_SCK (Audio interface as slave)	2	-	ns
t_{h_SCK}	Input Hold Time from AO_SCK (Audio interface as slave)	2	-	ns
$t_{ws(SCK)}$	AO_SCK to AO_WS	-	10	ns

13.10 Sony Philips Digital Interface (SPDIF) timing

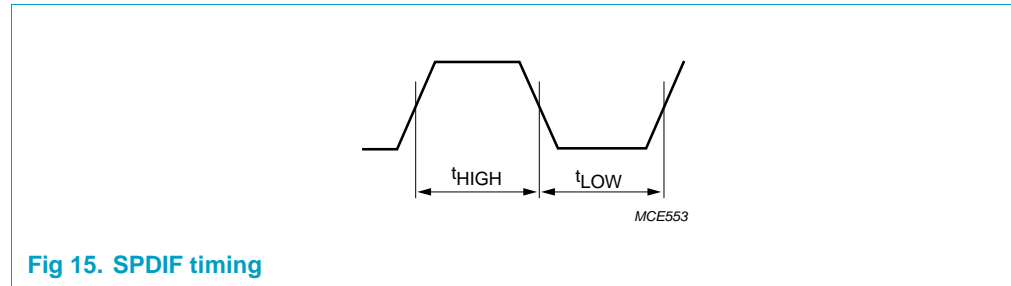


Fig 15. SPDIF timing

Table 33: SPDIF timing

Symbol	Parameter	Min	Typical	Max	Unit
t_{HIGH}	CLK High Time (PCI)	-	5.2	-	μ S
t_{LOW}	CLK Low Time (PCI)	-	5.2	-	μ S

13.11 Digital Video Output (DV Out) timing

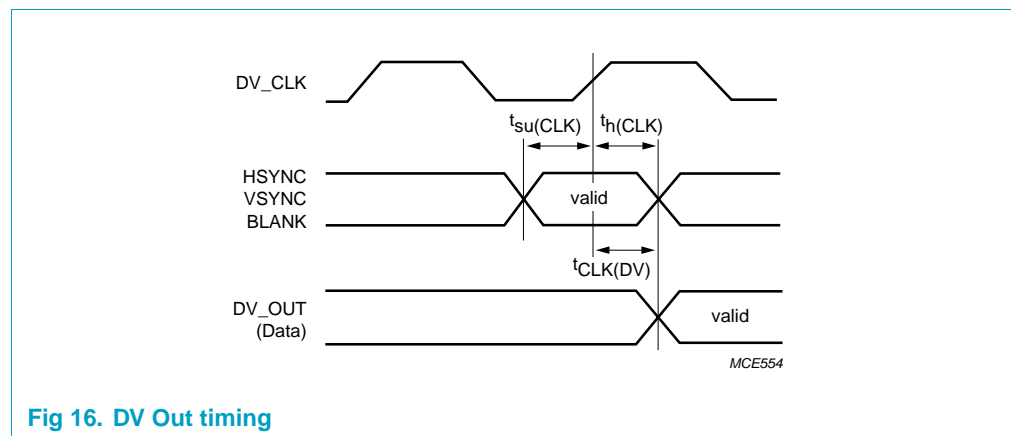


Fig 16. DV Out timing

Table 34: DV Out timing

Symbol	Parameter	Min	Max	Unit
DV_CLK	Video out clock frequency	27	-	MHz ^[1]
$t_{CLK(DV)}$	DV_CLK to DV_OUT	-3.7	0	ns
$t_{su(CLK)}$	VSYNC Setup Time to DV_CLK (as input)	3	-	ns
$t_{h(CLK)}$	CRT Control Hold Time from DV_CLK HSYNC, VSYNC, BLANK	0	-	ns

[1] DV_CLK period is programmable via the internal PLL

13.12 Digital Video Input (DV Input) timing

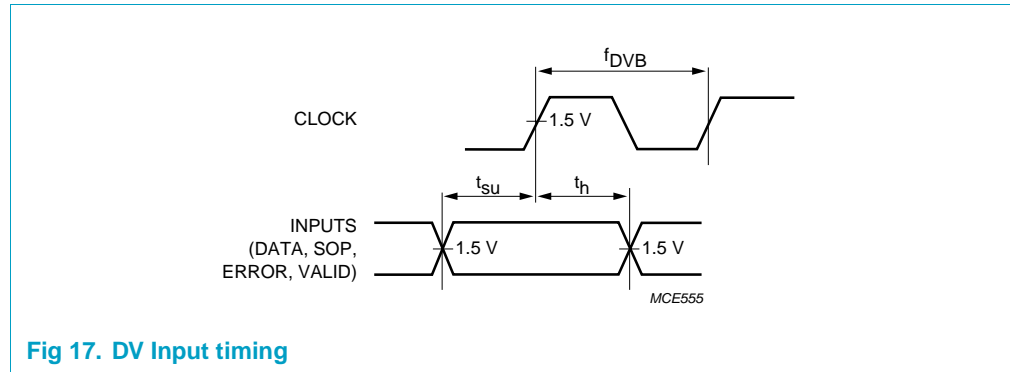


Fig 17. DV Input timing

Table 35: DV Input timing (VDICLK-referenced)

Symbol	Parameter	Min	Typical	Max	Unit
t_{su}	[7:0] setup	3	-	-	ns
t_h	[7:0] hold	3	-	-	ns
f_{DVB}	Clock	-	27	-	MHz

13.13 Transport Stream Output (TSO) timing

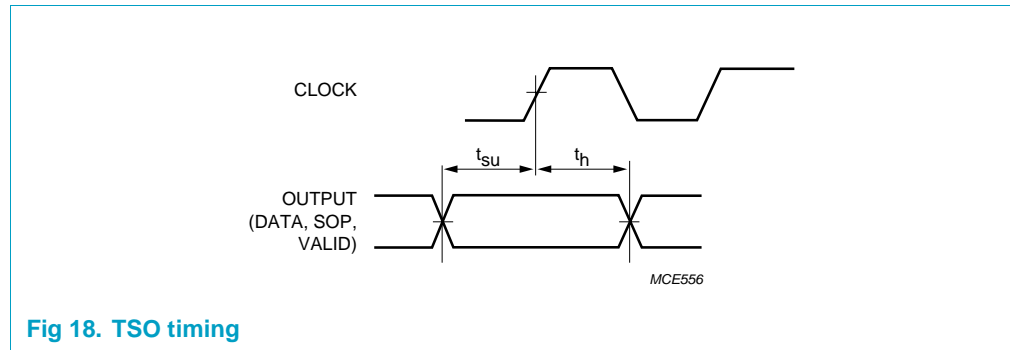


Fig 18. TSO timing

Table 36: TSO timing

Symbol	Parameter	Min	Typical	Max	Unit
t_{su}	Data setup	3	-	-	ns
t_h	Data hold	0	-	-	ns

13.14 JTAG test contacts

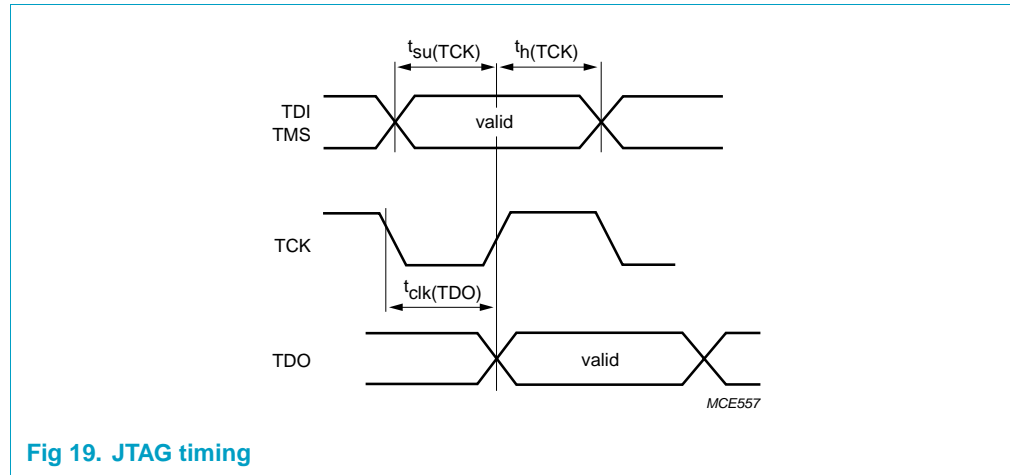


Fig 19. JTAG timing

Table 37: JTAG timing

Symbol	Parameter	Min	Max	Unit
$t_{clk(TDO)}$	JTAG_TCK to JTAG_TDO Valid delay	TBD		
$t_{su(TCK)}$	Input Setup Time JTAG_TCK	TBD		
$t_h(TCK)$	Input Setup Time JTAG_TCK	TBD		

14. Delta compared to PNX8525

There are a number of differences between the PNX8526 and the PNX8525 with respect to the physical interfacing of the device. These differences are described in [Table 38](#).

Table 38: Differences - 8525 / 8526

Characteristic	PNX8525	PNX8526
Core supply voltage	1.8 V ± 5%	1.26 V ± 0.06 V
I2C-bus pads	GPIO pads with schmitt trigger and pull-ups	Special I ² C pads designed to meet the I ² C specification
IEEE-1394 pads	GPIO pads with schmitt trigger and pull-ups	Special IEEE-1394 pads designed to meet the IEEE-1394 Link to Phy specification
PCI Interface	Supports 5 V tolerant interface with 3.3 V signalling	No 5 V tolerant interface, all signals limited to 3.3 V
System reset output (SYS_RSTN_OUT)	Drive capability 12 mA	Drive capability 8 mA
Clock output (PLL_OUT)	Drive capability 12 mA	Drive capability 8 mA
SPDIF output		

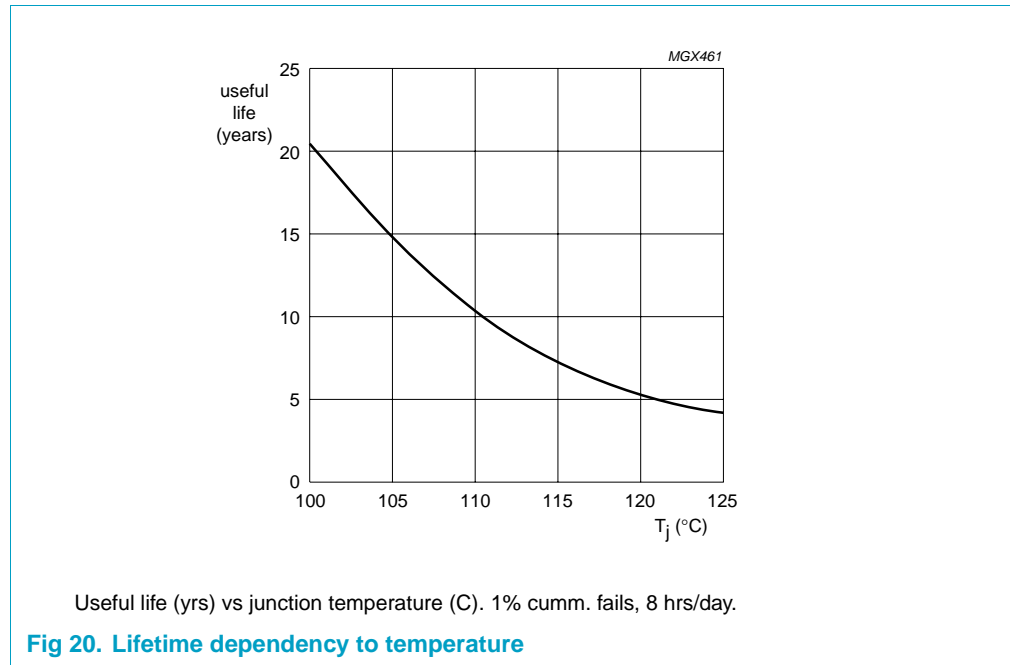
Table 38: Differences - 8525 / 8526...continued

Characteristic	PNX8525	PNX8526
	Drive capability 16 mA	Drive capability 14 mA
DV1 port, SSI, Uart2, Smart Card1, Smart Card2		
	Drive capability 4 mA	Drive capability 5 mA, INputs support Hysteresis
I2S CLK and WS		
	Drive capability 4 mA	Drive capability 5 mA
TS interface and I2S data lines		
	Hysteresis on inputs not supported	Hysteresis on inputs supported
SDRAM interface		
	Supports 5 V tolerant signalling, with 3.3 V drive. (AD[11:0],CLK[1:0], RAS,CAS, CS, BA[1:0] have drive capability 16 mA)	No 5 V tolerant signalling. Drive capability 14 mA
XIO SEL[2:0], ACK, A25		
	Drive capability 12 mA	Drive capability 8 mA
Peripheral power supply		
	Single connection on PCB for all V_{DD} bondpads	Requires separation of V_{DDC} into 3 segments, each segment filtered and star connected back to source. ^[1]
Core power supply		
	Single connection on PCB for all V_{DDC} bondpads	Requires separation of V_{DDC} into 2 segments, each segment filtered and star connected back to source. ^[2]

- [1] The new connections are
 V_{DD1} - The I/O supply connection
 V_{DD2} - Analogue clock generation unit (CAB-Custom Analogue Block)
 V_{DD3} - Trimedia™ clock generation PLL
- [2] The new connections are
 V_{DDC1} - Main core supply connection
 V_{DDC2} - 1.728GHz PLL supply connection

15. Lifetime versus temperature

The relationship between operating (junction) temperature and the expected lifetime of a device is shown in [Figure 20](#).



Referring to **Figure 20**, at a junction temperature of 110 °C a 10 year lifetime can be expected (8 hours/day). If increased to 125 °C, lifetime can be reduced to 4 years. Junction temperature can be influenced by following the guidelines in **Section 11**.

16. Package outline

HBGA456: plastic thermal enhanced ball grid array package; 456 balls;
body 35 x 35 x 1.8 mm; heatsink

SOT610-1

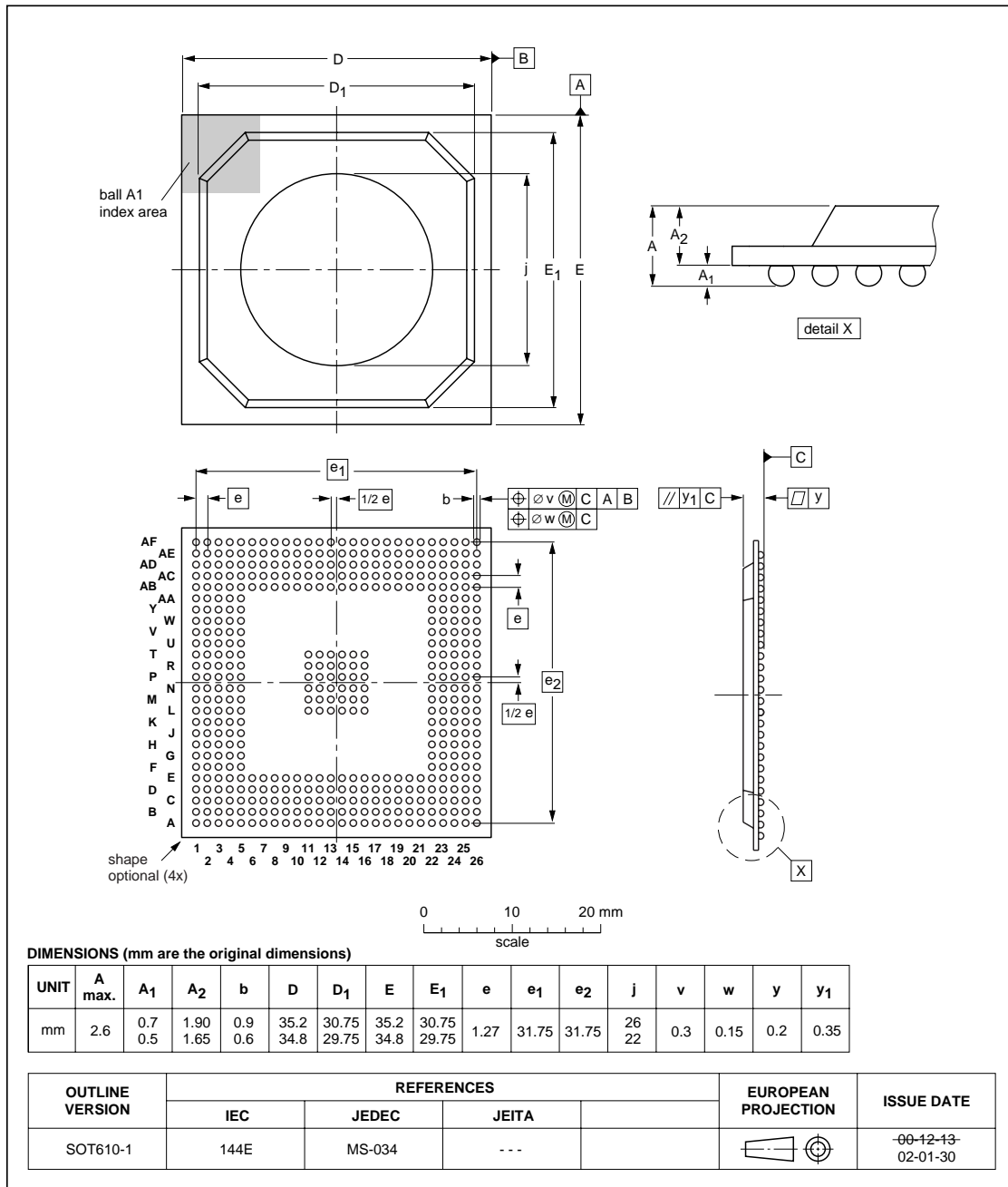


Fig 21. HBGA package outline

17. Soldering

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA and SSOP-T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Package related soldering information

Table 39: Suitability of surface mount IC packages for wave and reflow soldering methods

Package ^[1]	Soldering method	
	Wave	Reflow ^[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T ^[3] , TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ^[4]	suitable
PLCC ^[5] , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ^{[5][6]}	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ^[7]	suitable
PMFP ^[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding $217\text{ °C} \pm 10\text{ °C}$ measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Hot bar or manual soldering is suitable for PMFP packages.

18. Revision history

Table 40: Revision history

Rev	Date	CPCN	Description
01	20031006	-	Preliminary data (9397 750 11715)

19. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
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Contents

1	General description	1	21	Disclaimers	58
2	Features	2	22	Licenses	58
3	Applications	2	23	Trademarks	58
4	Ordering information	2	24	Contact information	58
5	Block diagram	3			
6	Pinning information	4			
6.1	Pinning	4			
6.2	Pin description	4			
6.2.1	Multi-function pins	30			
7	Functional description	37			
8	I/O multiplexer control register	39			
9	Power supply sequencing	40			
9.1	Power on sequence	40			
9.2	Power off sequence	41			
10	Limiting values	41			
11	Thermal characteristics	41			
12	Static characteristics	42			
13	Dynamic characteristics	43			
13.1	Reset timing	43			
13.2	Peripheral Controller Interface (PCI) timing	43			
13.3	Main Memory Interface (MMI) timing	45			
13.4	General Purpose Input/Output (GPIO) timing	45			
13.5	Universal Asynchronous Receiver/Transmitter (UART) timing	46			
13.6	Synchronous Serial Interface (SSI) timing	46			
13.7	I ² C-bus timing	47			
13.8	IEEE 1394 Phy-Link interface	47			
13.9	I2S audio input & output timing	48			
13.10	Sony Philips Digital Interface (SPDIF) timing	49			
13.11	Digital Video Output (DV Out) timing	49			
13.12	Digital Video Input (DV Input) timing	50			
13.13	Transport Stream Output (TSO) timing	50			
13.14	JTAG test contacts	51			
14	Delta compared to PNX8525	51			
15	Lifetime versus temperature	52			
16	Package outline	54			
17	Soldering	55			
17.1	Introduction to soldering surface mount packages	55			
17.2	Reflow soldering	55			
17.3	Wave soldering	55			
17.4	Manual soldering	56			
17.5	Package related soldering information	56			
18	Revision history	57			
19	Data sheet status	58			
20	Definitions	58			



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